Chapter 25
Data–Stream–Driven Computers are Power and Energy Efficient

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ABSTRACT

It is believed that data-stream-driven computing is power and energy efficient as compared to its counterpart, instruction-stream-driven computing. This latter requires memory access and memory control overheads while the processor is fetching task instructions from the memory. The programmer describes all the tasks as instructions in the program memory. On the other hand data-stream-driven computer is already configured or hardwired for a specific computing operation, no memory is required apart from data storage. In some contexts we refer to data-stream-driven computers as accelerators or single-purpose processors. This chapter discusses the benefit of data-stream-driven computing for better power and energy efficiency. We took matrix multiplication as an example application to compare the power and energy dissipations between load/store and non-instruction fetch-based architectures. We witnessed that single-purpose processor reduces almost 100% of the dynamic power when replacing the general-purpose processor. With the current mainstream transistor technology, morphware platforms that allow massive parallelism are the potential key for data-stream-driven computer implementations to saving energy in battery-powered embedded systems and to solve the dissipated power dilemma, as the heat becomes the bottleneck of traditional high frequency processors. If the same strategy is applied to mainstream computers and data center servers, we will not only reduce electricity bills but we will also contribute to greener computing by lowering the IT sector's CO_2 emissions.

INTRODUCTION

There exist two design models of general-purpose machine, the first one is called von Neumann, which uses the same memory for program and Data, the second model is called Harvard which uses separate memories for program and Data. Both models share the same characteristic for being general to execute the instructions residing in the program memory. High speed and multiple-cores CPU does not necessarily ensure fast program execution, as the execution is limited by the speed of data and instruction, which are exchanged between the processor and the memory. An astronomic program causes a massive overhead due to load/store routines, this is the von Neumann bottleneck. High speed and multiple-cores CPU signify directly high power consumption, as the dissipated power is proportional to the clock frequency. Memory access manifests to a significant portion of power dissipation due to the switching activities in data and address lines and other memory handling logic. On the other hand special HW or single-purpose machine does not need a program memory and therefore no instructions fetch is required, tasks are performed as soon as data is available. Although, both general and single-purpose processors kept their places in the computing area, with today's technology trends, the general-purpose processor is losing its dominance by the important presence of reconfigurable technology, which allows constructing single-purpose processors on the fly. In this chapter we will examine the effect of configured dedicated HW on power and energy saving when replacing the general-purpose processor.

RELATED WORK

Comparing single-purpose and general-purpose processors for power, energy and latency has been addressed in many literatures, however we hope that further reporting may yet push the message

for reaching decision makers and other involved communities.

Azzopardi, Vanderbauwhede and Moadeli (2009) raised the need of green computing systems for large data processing, they demonstrated that data-stream-driven computers on FPGAs have a potential for environment friendly computing. Their demonstration consists of comparing power and energy consumption when a documents filtering algorithm is implemented in both architectures. The algorithm consumes about 130W when employing instruction fetch-based design on a dual-core Itanium 64-bit processor running at 1.6GHz, on the other hand it consumes 1.25 watts only when employing non-instruction based design on the FPGAs platform using Virtex-4 FPGAs.

Thomas, Howes, and Luk (2009) compared the power efficiency in four different types of platform when implementing three methods of random number generations, the platforms in question are: conventional multi-core CPUs (Intel Core2), GPUs (Nvidia GTX 200), FPGAs (Xilinx Virtex-5) and MPPAs (Massively Parallel Processor Arrays) (Ambric M2000). Their finding shows that non-instruction fetch-based design on FPGAs platform has the best power efficiency with 1461.20 Msapmle/Joule (millions of samples per joule), followed by MPPAs with 150.21 MSample/Joule and GPUs with 114.55 MSample/Joule, while the multi-core CPUs led to the worst case of power efficiency with only 5.07 MSample/Joule. The figures are the average power efficiency between the three methods of random number generation, the uniform, the Gaussian and the exponential.

Single-purpose processors have been used to speed up computing in many different areas such as data mining, bioinformatics and space engineering, Baker and Parsanna (2005) employed reconfigurable technology for implementing the systolic array architecture using single-purpose processors, the implementation shown a significant performance improvement as compared to the state-of-the-art SW implementation, Harris, Jacob,

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