Chapter 3
Machine Intelligence Using Hierarchical Memory Networks

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ABSTRACT

This chapter presents the fundamentals of a hardware based memory network that can perform complex cognitive tasks. The network is designed to provide space dimensionality reduction, which enables desired functionality in a random environment. Complex network functionality is achieved by simple network cells that minimize the needed chip area for hardware implementation. Functionality of this network is demonstrated by automatic character recognition with various input deformations. In the character recognition, the network is trained to recognize characters deformed by random noise, rotation, scaling, and shifting. This example demonstrates how cognitive functionality of a hardware network can be achieved through an evolutionary process, as distinct from design based on mathematical formalism.

INTRODUCTION

Computational, cognitive and memory capability of human brain has inspired researchers to emulate brain function or capability in artificial intelligent systems (D. D. Nolte 2001;S. Engelmann et al 2004;A. Konar 2000; D. M. Gabbay etal 1998;J. J. Hopfield etal 1986; A. Hjelmfelt etal 1993). The artificial intelligent systems are implemented in software or hardware and often derived from mathematical or logical modeling of brain capability, examples of which are Artificial Neural Networks (ANN), Fuzzy Logic, Evolutionary computation, Bayesian networks, Expert systems, case based reasoning and behavior based artificial intelligence. They find application in knowledge based problems, pattern recognition problems, optimization problems and adaptive control problems (J. J. Hopfield 1986; A. Hjelmfelt 1993;M. Tzanakou et al 2000;S. K. Pal etal 2001; J. R. Leigh 2004; S. S. Rao 1996;J. J. Hopfield 1988; M. Valle 2002; G. Ascia etal 1999; S. Bouras et al 1998). Hardware chips have many advantages over software implementations, but the existing hardware implementations are limited to low functional complexity and small

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number of inputs. As an example for large input problem, ANN architecture needs many neural nodes and weights which requires many amplifiers and memory elements (R. Mason etal 1992; L. O. Chua 2002). Large area is needed to place these components and with increase in number of neural nodes the number of interconnections between the neural nodes between different layers becomes high. This results in impossible cell routing in a limited chip area, while large area requirement of the amplifiers and memory elements limit the size of the network (L. O. Chua 2002; S. Balkir 2003;A. A. Stocker 2006;T. Oohori et al. 2007). Similarly FL chip implementation with large number of inputs is also not possible due to hardware complexity. In this book chapter, we present the concept of hardware-based memory network (A. P. James, 2010) that can perform cognitive tasks. The functionality of the network is demonstrated by a challenging example of character recognition with applied input deformations.

NETWORKS IN INFORMATION PROCESSING

Complex networks such as neural networks and cognitive memory networks can be classified as a network based approach to information processing, often finding its way in formulating interrelationships within an intelligent systems framework. The ability of making decisions is the key aspect in understanding the interpretation drawn from the network analysis. Clearly, information as we know today is a concept that is perceived to be useful to make informed judgments at local and global decision levels. The hierarchical processing of information is a unique and interesting aspect of the human brain, which is by at large implemented in the layered structure of the cortex. Each module in a human brain has evolved in structure and is trained to process and understand the information specific to a given task. The interaction between the modules results in the ability of the human brain to understand and respond to the complex cognitive task. The interaction of the module follows a hierarchical organization, where sensory processes can be visualized as the bottom part of the hierarchy and decision making processes can be visualized as the top most part of the hierarchy. This talk provides insights into the new paradigm of thinking in machine based information processing methods. In this chapter, we present the very ideas of human intelligence in perspective of semiconductor memory elements that can be used for creating real-time intelligent information procession units and systems.

The perceived idea of what is accurate "information" in a process is independent of the source but is dependent on the nature of training undergone to the cortical neural network. The cortical network in the brain embodies several interesting concepts such as modularity, hierarchy, and sparse representation. Modularity has drawn several analogies to the human mind, wherein the module can be considered as an intelligent subsystem for perception, where they remain independent of the overall functionality of perception, thus they can be viewed as encapsulated information. Along with perceptual modularity, one can also observe structural modularity of the human brain, with every part of human brain having a different arrangement of neurons inheriting different types of functionality. Hierarchy is implicit to a modular system, and has been argued to be integral to the working of the human brain. The structural hierarchy as well as the functional hierarchy in human brain makes it very unique and different from that of a typical machine based system. Recently, however the idea of hierarchy was seen not to be universal to brain, as more complex functionalities followed rather closely to a network topology. Sparse representation makes the information processing very interested in the human brain, as it tries to organize the information into something meaningful and relevant to the events that capture the attention of an event. This is by far very different from the way information

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