

Chapter 18

Reducing Design Margins by Adaptive Compensation for Thermal and Aging Variations

Zhenyu Qi

University of Virginia, USA

Yan Zhang

University of Virginia, USA

Mircea Stan

University of Virginia, USA

ABSTRACT

Corner-based design and verification are based on worst-case analysis, thus introducing over-pessimism and large area and power overhead and leading to unnecessary energy consumption. Typical case-based design and verification maximize energy efficiency through design margins reduction and adaptive computation, thus helping achieve sustainable computing. Dynamically adapting to manufacturing, environmental, and usage variations is the key to shaving unnecessary design margins, which requires on-chip modules that can sense and configure design parameters both globally and locally to maximize computation efficiency, and maintain this efficiency over the lifetime of the system. This chapter presents an adaptive threshold compensation scheme using a transimpedance amplifier and adaptive body biasing to overcome the effects of temperature variation, reliability degradation, and process variation. The effectiveness and versatility of the scheme are demonstrated with two example applications, one as a temperature aware design to maintain I_{ON} to I_{OFF} current ratio, the other as a reliability sensor for NBTI (Negative Bias Temperature Instability).

INTRODUCTION

IT infrastructure has become an essential foundation of human society. Information storage and computation span every aspect of our daily life, from personal entertainment and education, to

government and business operation. Moreover, for real-time service providers, data centers and their connections to outside terminals need to be running for a long time without interruption. Examples are banking systems and servers, online shopping and tracking, supply chain management, and multimedia streaming. The unprecedented increasing dependence and requirement on transaction avail-

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ability and speed call for the deployment of more high performance and reliable computing devices.

However, this leads to at least two problems. At the macroscale level, without careful design and planning the environmental impact due to technology development is unsustainable. For example, the energy cost of IT infrastructure and its carbon footprint doubles in less than five years (Pedram, 2009). Technology-equipped buildings occupy 70% of total electricity usage and emit 40% of greenhouse gases annually in the US (Kleissl & Agarwal, 2010). At the microscale level, high performance and reliability could be at odds for concurrent circuit designs based on the semiconductor technology. For example, high performance designs usually come with high power/temperatures and high stress levels on devices, leading to thermal and reliability problems. In particular, they can cause the instability (including both short time variation and long time shifting) of the threshold voltage of the basic circuit element—CMOS transistors.

The threshold voltage, or V_{TH} , is a critical parameter in circuit design. V_{TH} determines the current flowing through the transistor at least linearly, and in turn affects its equivalent resistance, transconductance, pull-up or pull-down strength and ultimately the speed and power of circuits. Even in advanced sub-micron technologies the dependence of the transistor current on V_{TH} can still be quite super-linear when all short channel effects are considered (Qi & Stan, 2007). The effects in the sub-threshold region are even more prominent since the leakage current grows exponentially as V_{TH} decreases.

Although threshold voltages are specified by technology vendors and treated as fixed and static values in simulations at design time, run-time factors like temperature variability and reliability degradation, as well as process variation, can considerably change V_{TH} both in the short and long term for individual transistors. With the small margins of most circuit designs today, even a relatively small amount of shift can have a sig-

nificant impact or even lead to circuit failure. On the other hand, preventing these failures by initial overdesigning with large upfront built-in margins can impose large penalties in area and power. For example, an optimized reliability-aware sizing algorithm proposed in (Paul, Kang, Kufluoglu, Ashraful Alam, & Roy, 2006) still incurs an area overhead from 3.31%-13.6% for ISCAS testbench circuits. This conventional method variation by overdesign to tolerate reliability hazards, thermal issues and process leads to unsustainable increase of cost both for the designer and the users.

In this chapter, we propose an adaptive threshold compensation scheme using a transimpedance amplifier and adaptive body biasing to compensate the V_{TH} shift dynamically. The effect of body biasing on modulating transistor threshold voltages has been heavily exploited in recent years to achieve low power and combat process variation (Karnik, Borkar, & De, 2002; Tschanz, et al., 2002). The scheme employed in this chapter works for a range of applications including, but not limited to, manufacturing process variations. Two example applications are presented in this chapter. The first compensates for temperature induced I_{ON} to I_{OFF} mismatch and the second compensates for threshold shifting due to the long time aging/reliability effect.

Adaptive compensation of threshold voltage reduces necessary design margins, and enables typical case-based design instead of the traditional worst case-based (or corner based) design. Worst case-based design leads to over-pessimism and unnecessarily large margins/guardbands for the majority of components that do not fall on the tail of the distribution caused by manufacturing or runtime variations. The over-designed components not only take chip real estate and impose non-recurring penalty for designers and manufacturers, but also consume extra power and impose a recurring penalty on the consumer and the environment. The proposed module can also be deployed in large numbers and distributed across the whole chip for adaptive compensa-

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