Chapter 14
Structural Outlooks for the OTIS-Arrangement Network

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ABSTRACT

Recent studies have revealed that the Optical Transpose Interconnection Systems (OTIS) are promising candidates for future high-performance parallel computers. This paper presents and evaluates a general method for algorithm development on the OTIS-Arrangement network (OTIS-AN) as an example of OTIS network. The proposed method can be used and customized for any other OTIS network. Furthermore, it allows efficient mapping of a wide class of algorithms into the OTIS-AN. This method is based on grids and pipelines as popular structures that support a vast body of parallel applications including linear algebra, divide-and-conquer types of algorithms, sorting, and FFT computation. This study confirms the viability of the OTIS-AN as an attractive alternative for large-scale parallel architectures.

INTRODUCTION

The choice of network topology for parallel systems is a critical design decision that involves inherent trade-offs in terms of efficient algorithms support and network implementation cost. For instance, networks with large bisection width allow fast and reliable communication. However, such networks are difficult to implement using today's electronic technologies that are two dimensional in nature (Wang & Sahni, 2002). In principle, free-space optical technologies offer several fronts to improve this trade-off. The improved transmission rates, dense interconnects, power consumption, and signal interference are few examples on these fronts (Agelis, 2005; Akers et al., 1977; Dally,

DOI: 10.4018/978-1-4666-2065-0.ch014

1988; Day & Tripathi, 1990; Hendrick et al., 1959; Wang & Sahni, 2001; Yayla et al., 1998).

In this paper, we focus on Optical Transpose Interconnection Systems Arrangement Networks-(OTIS-AN) which was proposed by Al-Sadi that can be easily implemented using free-space optoelectronic technologies (Agelis, 2005; Al-Sadi & Awwad, 2010). In this model, processors are partitioned into groups, where each group is realized on a separate chip with electronic inter-processor connects. Processors on separate chips are interconnected through free space interconnects. The philosophy behind this separation is to utilize the benefits of both the optical and the electronic technologies.

The advantage of using OTIS as optoelectronic architecture lies in its ability to maneuver the fact that free space optical communication is superior in terms of speed and power consumption when the connection distance is more than few millimeters (Dally, 1988). In the OTIS-AN, shorter (intra-chip) communication is realized by electronic interconnects while longer (inter-chip) communication is realized by free space interconnects.

Extensive modeling results for the OTIS have been reported in (Day & Tripathi, 2002). The achievable Terra bit throughput at a reasonable cost makes the OTIS-AN a strong competitive to the to its factor network (Dally, 1988; Krishnamoorthy et al., 1992; Marsden et al., 1993).

These encouraging findings prompt the need for further testing of the suitability of the OTIS-AN for real-life applications. A number of recent studies have been conducted in this direction (Al-Sadi, 2004; Awwad & Al-Ayyoub, 2001; Chatterjee & Pawlowski, 1999; Day & Al-Ayyoub, 2002). Awwad (2005) have presented and evaluated various algorithms on OTIS-networks such as basic data rearrangements, routing, selection and sorting. They have also developed algorithms for various matrix multiplication operations and image processing (Sahni & Wang, 1997; Wang & Sahni, 2000). Zane et al. (2000) have shown that the OTIS-mesh efficiently embeds four-dimensional meshes and hypercubes.

Aside from the above mentioned works, the study of algorithms on the OTIS is yet to mature (Sahni, 1999). In this paper we contribute towards filling this gap by presenting a method for developing algorithms on the OTIS-AN. These methods is based on grid and pipeline as popular a structure that supports a vast body of applications ranging from linear algebra to divide-and-conquer type of algorithms, sorting, and FFT computation. The proposed methods are discussed in the sequel, but first we give the necessary definitions and notation

PRELIMINARY NOTATIONS AND DEFINITIONS

Let n and k be two integers satisfying $1 \leq k \leq n$-1 and let us denote $<n> = \{1, 2,\ldots, n\}$ and $<k> = \{1, 2,\ldots, k\}$. Let P_k^n taken k at a time, the set of arrangements of k elements out of the n elements of $<n>$. The k elements of an arrangements p are denoted $p_1, p_2,\ldots, p_k$.

Definition 1 (Arrangement Graph)**:**

The (n,k)-arrangement graph $A_{n,k} = (V, E)$ is an undirected graph given by:

$V= \{ p_1p_2\ldots p_k | p_i \text{ in} <n> \text{ and } p_i \neq p_j \text{ for } i \neq j\} = P_k^n$, …. (1)

and

$E = \{(p,q) \mid p \text{ and } q \text{ in } V \text{ and for some } i \text{ in } <k>, p_i \neq q_i \text{ and } p_j = q_j \text{ for } j \neq i\}$. … (2)

That is the nodes of $A_{n,k}$ are the arrangements of k elements out of n elements of $<n>$, and the edges of $A_{n,k}$ connect arrangements which differ exactly in one of their k positions. For example in $A_{5,2}$ the node p=23 is connected to the nodes 21, 24, 25, 13, 43, and 53. An edge of $A_{n,k}$ connect-