

Chapter 4

Dynamic Thermal Management for Multi- / Many-Core Systems

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ABSTRACT

High chip complexity and power consumption raise chip temperature, reduce lifetime, affect the reliability, and increase the cooling cost. Dynamic Thermal Management (DTM) techniques are design to control the chip temperature and tackle the thermal related issues. In this chapter, the authors introduce the working principles and implementation details of some state-of-the-art DTM techniques, in order to boost thermal awareness in the green computing community. They first give the motivation of dynamic thermal management, and divide existing DTM approaches into different categories based on their characteristics. Then the detailed design and implementation issues of these techniques are carefully discussed. Finally, the authors share future research directions in this area.

1. INTRODUCTION

Moore's law states that the number of transistors on a chip doubles about every two years or less. As we continue to shrink the chip sizes and extract the performance of our systems at the cost of higher power consumption, the ever-increasing chip complexity and power density elevate peak temperatures of the chip and imbalance the thermal

gradients. Raised peak temperatures reduce the lifetime of the chip, deteriorate its performance, affect the reliability, and increase the cooling cost (Skadron, Stan, Sankaranarayanan, Huang, Velusamy, & Tarjan, 2004). The adverse positive feedback between leakage power and raised temperature creates the potential of thermal runaway. When mapped on a multi or many-core system, the diverse workload of applications may lead to power and temperature imbalance among different cores. Such temporal and spatial variation in

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temperature creates local temperature maxima on the chip called the hotspot (Donald & Martonosi, 2006). An excessive spatial temperature variation, which is also referred to as the thermal gradient, increases clock skews and decreases performance and reliability. Elevated temperatures require more cooling efforts; to cool down the processor, a typical cooling fan can consume up to 51% power budget of a server (Lefurgy, Rajamani, Rawson, Felter, Kistler, & Keller, 2003; Ayoub, Sharifi, & Rosing, 2010).

Dynamic Thermal Management (DTM) techniques are designed to tackle the aforementioned problems and control the chip temperature as well as power consumption. As long as the temperature is regulated, the system reliability can be improved significantly. It has been pointed out that a moderate reduction in temperature by 10°C~15°C can extend the lifespan of the electronic device 2 times (Kursun, Cher, Buyuktosunoglu, & Bose, 2006), and 10°C decrease in the magnitude of thermal cycles can achieve 16 times increase in mean time to failure for metallic structures. Leakage power also drops significantly when temperature reduces. For every 9° C temperature reduction, there is 50% reduction in the leakage power (Liu, Dick, Shang, & Yang, 2007). This reduction is particularly important in the future System-on-Chip design, because the leakage power consumption is estimated to account for more than 50% of total chip power consumption (Semiconductor Industry Association, 2001). Regulated temperature not only guarantees the system reliability and reduces leakage power consumption, but also boosts the performance. Transistor switching speed is faster in low temperature (Pamula & Chakrabarty, 2003). A balanced spatial gradient can mitigate the clock skew problem noticeably.

The goal of this book chapter is to provide the audience a thorough understanding of the working principles and implementation details of some state-of-the-art Dynamic Thermal Manage-

ment (DTM) techniques, and to boost the thermal awareness in the green computing community. We will first give the motivation of dynamic thermal management, then present a detailed survey on some existing DTM approaches with detailed discussions on common design and implementation issues, and finally share our view in the future research directions in this area.

2. BACKGROUND

2.1. An Overview of Dynamic Thermal Management Techniques

Dynamic thermal management refers to those techniques that enable the chip to autonomously modify the task execution and power dissipation characteristics so that the lower-cost cooling solutions could be adopted while still guaranteeing safe temperature regulation. A DTM controller observes system information during runtime and takes thermal management actions accordingly. It maintains the system temperature below a safe threshold or reduces thermal violations as much as possible with minimum performance overhead.

The most important system information that is required to carry out the dynamic thermal management for a computing system is the chip temperature. This information can be read from the on-chip temperature sensors or estimated using a thermal model. In addition to the temperature information, application characteristics, task power consumptions, etc. are also needed by some state-of-the-art DTM techniques.

A great number of different dynamic thermal management actions have been investigated. These actions include clock gating, dynamic voltage frequency scaling, computation migration and hybrid methods, which combine two or more techniques mentioned above. Although different techniques use different mechanisms and are ap-

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