

Chapter 2.23

A Biomimetic Adaptive Algorithm and Micropower Circuit Architecture for Implantable Neural Decoders

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ABSTRACT

Algorithmically and energetically efficient computational architectures that operate in real time are essential for clinically useful neural prosthetic devices. Such architectures decode raw neural data to obtain direct motor control signals for external devices. They can also perform data compression and vastly reduce the bandwidth and consequently power expended in wireless transmission of raw data from implantable brain-machine interfaces.

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We describe a biomimetic algorithm and micropower analog circuit architecture for decoding neural cell ensemble signals. The decoding algorithm implements a continuous-time artificial neural network, using a bank of adaptive linear filters with kernels that emulate synaptic dynamics. The filters transform neural signal inputs into control-parameter outputs, and can be tuned automatically in an on-line learning process. We demonstrate that the algorithm is suitable for decoding both local field potentials and mean spike rates. We also provide experimental validation of our system, decoding discrete reaching

decisions from neuronal activity in the macaque parietal cortex, and decoding continuous head direction trajectories from cell ensemble activity in the rat thalamus. We further describe a method of mapping the algorithm to a highly parallel circuit architecture capable of continuous learning and real-time operation. Circuit simulations of a subthreshold analog CMOS instantiation of the architecture reveal that its performance is comparable to the predicted performance of our decoding algorithm for a system decoding three control parameters from 100 neural input channels at microwatt levels of power consumption. While the algorithm and decoding architecture are suitable for analog or digital implementation, we indicate how a micropower analog system trades some algorithmic programmability for reductions in power and area consumption that could facilitate implantation of a neural decoder within the brain. We also indicate how our system can compress neural data more than 100,000-fold, greatly reducing the power needed for wireless telemetry of neural data.

INTRODUCTION

Brain-machine interfaces have proven capable of decoding neuronal population activity in real time to derive instantaneous control signals for prosthetics and other devices. All of the decoding systems demonstrated to date have operated by analyzing digitized neural data (Chapin, Moxon, Markowitz, & Nicolelis, 1999; Hochberg et al., 2006; Jackson, Mavoori, & Fetz, 2006; Musallam, Corneil, Greger, Scherberger, & Andersen, 2004; Santhanam, Ryu, Yu, Afshar, & Shenoy, 2006; Taylor, Tillery, & Schwartz, 2002; Wessberg et al., 2000). Clinically viable neural prosthetics are an eagerly anticipated advance in the field of rehabilitation medicine, and development of brain-machine interfaces that wirelessly transmit neural data to external devices will represent an important step toward clinical viability. The general model for such devices has

two components: a brain-implanted unit directly connected to a multielectrode array collecting raw neural data; and a unit outside the body for data processing, decoding, and control. Data transmission between the two units is wireless. A 100-channel, 12-bit-precise digitization of raw neural waveforms sampled at 30 kHz generates 36 Mbs⁻¹ of data; the power costs in digitization, wireless communication, and population signal decoding all scale with this high data rate. Consequences of this scaling, as seen for example in cochlear-implant systems, include unwanted heat dissipation in the brain, decreased longevity of batteries, and increased size of the implanted unit. Recent designs for system components have addressed these issues in several ways, including micropower neural amplification (Holleman & Otis, 2007; Wattanapanitch, Fee, & Sarpeshkar, 2007); adaptive power biasing to reduce recording power in multielectrode arrays (Sarpeshkar et al., 2008); low-power data telemetry (Ghovanloo & Atluri, 2007; Mandal & Sarpeshkar, 2007, 2008; Mohseni, Najafi, Eliades, & Wang, 2005); ultra-low-power analog-to-digital conversion (Yang & Sarpeshkar, 2006); low-power neural stimulation (Theogarajan et al., 2004); energy-efficient wireless recharging (Baker & Sarpeshkar, 2007); and low-power circuits and system designs for brain-machine interfaces (Sarpeshkar et al., 2008; Sarpeshkar et al., 2007). Power-conserving schemes for compressing neural data before transmission have also been proposed (Olsson III & Wise, 2005). However, almost no work has been done in the area of power-efficient neural decoding (Rapoport et al., 2009).

Direct and power-efficient analysis and decoding of analog neural data within the implanted unit of a brain-machine interface could facilitate extremely high data compression ratios. For example, the 36 Mbs⁻¹ required to transmit raw neural data from 100 channels could be compressed more than 100,000-fold to 300 bs⁻¹ of 3-channel motor-output information updated with 10-bit precision at 10 Hz. Such dramatic compression brings

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