

Chapter 11

Intrinsic Evolvable Hardware Structures

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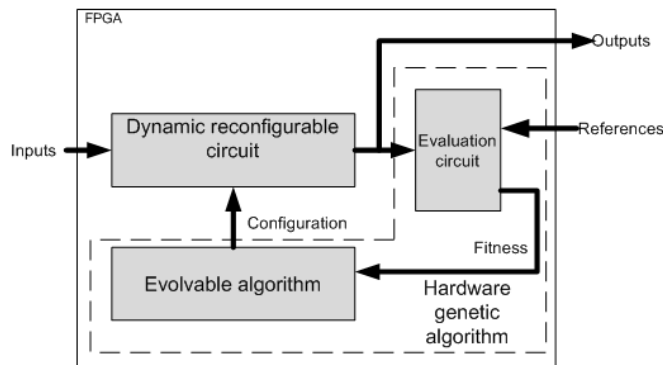
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ABSTRACT

The main target of this chapter is to present the intrinsic evolvable hardware structures: concept, design and applications. The intrinsic evolvable hardware structures concept join more research areas like: bio-inspired searching methods (evolutionary algorithms), optimization of algorithms by parallel processing and reconfigurable circuits. First, a general overview about intrinsic evolvable hardware structure is presented. The intrinsic evolvable hardware structure consists of two main modules: hardware genetic algorithm and dynamic reconfigurable circuit. The hardware genetic algorithm searches the configuration that makes the reconfigurable circuit to correctly respond to application requirements. The background section present the genetic algorithm concept as a bio-inspired search solution, the hardware reconfiguration concept with sub areas classifications and the research directions in the evolvable hardware structures areas with application examples. The main section presents the design solutions for hardware implementation of genetic algorithm and for the reconfigurable circuit. Finally, several applications are presented that illustrate the usefulness of the intrinsic evolvable hardware structure.

DOI: 10.4018/978-1-61520-893-7.ch011

Figure 1. Intrinsic evolvable hardware structure



INTRODUCTION

The reconfigurable hardware area, with one of its branches, evolvable hardware, is very dynamic and has experienced great developments in recent years. With 10 years ago from the time of writing the paper (2009) implementation of a logic circuit with a high degree of complexity on a programmable logic involves a series of problems caused by the limitation of existing technology. The market was dominated by complex programmable logic circuits and logic gates for areas of low resolution. Main problem was the number of available logic cells on the chip and response time. Extremely rapid evolution of technology has made at present on an area of programmable gate can be implemented a core processor for high speed, comparable in performance with versions of dedicated integrated circuits. Meanwhile the price of production has decreased very much what makes a modern configurable logic circuit to be available on the market. Therefore, it is necessary to have an evolution in design techniques, synthesis and implementation of logic circuits, techniques, still rely on classical logic programmable array. In those circumstances arise and develop areas of dynamic reconfigurable hardware with its new branch evolvable hardware. This tries to answer the question: in the context of current development of configurable logic circuits, it is

not possible to print a new direction in design, synthesis and implementation of logic circuits, so that performance is improved compared to classical methods? As in any new field, lines of research are multiple. One of the objectives of this work is to try to synthesis the assumptions made in a single theory concerning the evolutionary synthesis of logical circuits.

The starting point for this chapter is the intrinsic evolvable hardware structure (configurable through its own resources) illustrated in Figure 1.

It is composed of several modules, each allocate the sections in this chapter. A **reconfigurable circuit** is a circuit which can change their behavior according to a map of configurations that is generated.

The process of generating the map of connections, from a structural or functional description of the new behavior is called logic synthesis of the circuit. There are several classical methods for synthesis of logic circuits, but in principle the synthesis is a laborious process, requiring a high volume of operations (performed with the DeMorgan rules, minimization).

The evolutionary algorithms are search algorithms in an expanded space of multiple objective solutions. They are used in several areas in which other search methods are not effective. The use of evolutionary algorithms (EA) to solve multi objective problem has be motivated mainly

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