

## Chapter 27

# Configurable and Scalable Turbo Decoder for 4G Wireless Receivers

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### **ABSTRACT**

*The increasing requirements of high data rates and quality of service (QoS) in fourth-generation (4G) wireless communication require the implementation of practical capacity approaching codes. In this chapter, the application of Turbo coding schemes that have recently been adopted in the IEEE 802.16e WiMax standard and 3GPP Long Term Evolution (LTE) standard are reviewed. In order to process several 4G wireless standards with a common hardware module, a reconfigurable and scalable Turbo decoder architecture is presented. A parallel Turbo decoding scheme with scalable parallelism tailored to the target throughput is applied to support high data rates in 4G applications. High-level decoding parallelism is achieved by employing contention-free interleavers. A multi-banked memory structure and routing network among memories and MAP decoders are designed to operate at full speed with parallel interleavers. A new on-line address generation technique is introduced to support multiple Turbo interleaving patterns, which avoids the interleaver address memory that is typically necessary in the traditional designs. Design trade-offs in terms of area and power efficiency are analyzed for different parallelism and clock frequency goals.*

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## INTRODUCTION

The approaching fourth-generation (4G) wireless systems are promising to support very high data rates from 100 Mbps to 1 Gbps. This consequently leads to orders of complexity increases in a 4G wireless receiver. The high performance convolutional Turbo codes are employed in many 4G wireless standards such as IEEE 802.16e WiMax and 3GPP Long Term Evolution (LTE).

A Turbo decoder is typically one of the most computation-intensive parts in a 4G wireless receiver. Increased complexity and performance requirements and the need to reduce power and area are significant challenges for Turbo decoder hardware implementation. The push for multi-mode wireless physical layer (PHY) brings additional challenges for Turbo decoder design. While programmable DSP/SIMD/VLIW processors can offer great flexibility in supporting different types of Turbo codes, they have several drawbacks notably higher power consumption and lower throughput than the ASIC solutions, which make them unsuitable for handheld devices. The commonalities between these Turbo codes in 4G wireless standards allow resources to be shared thus reducing hardware area and making more efficient use of the data path. However, there are differences in the exact Turbo decoder implementations. In order to meet high-speed multiple 4G standards, a reconfigurable and scalable Turbo decoder (or coprocessor) is necessary. From an implementation point of view, there are many aspects of Turbo codes that make them still a very hot research topic. First, the original MAP algorithm is of great complexity, so it is impractical to implement it in hardware. So the Log-MAP

and Max-Log-MAP algorithms were proposed later to reduce the arithmetic complexity while still maintaining good decoding performance. The long latency of MAP decoding has prevented it from being used in the real-time systems. One effective solution is to apply a sliding window algorithm to reduce the decoding latency. The scheduling of parallel sliding windows becomes the main challenge in parallel Turbo decoder design. Second, the non-binary Turbo codes are proven to have better performance than the binary Turbo codes. An area-efficient high-radix Turbo decoder architecture poses another design challenge. Finally, the new contention-free interleaver enables a very high level of parallelism in Turbo decoding, but on the other hand it creates an obstacle for the internal memory structure. The memories need to be partitioned and managed properly to avoid memory access conflicts introduced by the interleaver.

This chapter discusses several types of Turbo coding schemes that have recently been approved in IEEE 802.16e WiMax, 3GPP LTE, and some other 3G/4G standards. It describes a high-throughput, area- and power- efficient VLSI architecture for multi-mode Turbo decoders. A multi-banked memory structure and routing network between memories and MAP decoder cores are also introduced. Simulation and implementation results are presented which show that, with the aid of a unified trellis structure, a configurable and scalable Turbo decoder architecture provides a practical solution to the requirements of flexible and high data-rate reliable transmission for 4G wireless networks.

Table 1. Some applications of Turbo codes

Application	Code structure	Polynomials
CDMA, WCDMA, UMTS, LTE	8-state binary	13, 15, 17
WiMax, DVB-RCS	8-state double-binary	15, 13

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