

Chapter 8

Teaching Principles of Petri Nets in Hardware Courses and Students Projects

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ABSTRACT

The paper presents the principles of using Petri Net formalism in hardware design courses, especially in the course “Architecture of peripheral devices”. Several models and results obtained by student individual or group projects are mentioned. First the using of formalism as a modeling tool is presented consecutively from Place/Transition nets to Coloured Petri nets. Then the possible Petri Nets using as a hardware specification for direct hardware implementation (synthesized VHDL for FPGA) is described. Implementation and simulation results of three directly implemented models are presented.

INTRODUCTION

Petri nets (PN) are a well established mechanism for system modeling. They are a mathematically defined formal model, and can be subjected to a large variety of systems. PN based models have been widely used due to their ease of understanding, declarative, logic based and modular modeling principles, and finally because they can be represented graphically. Since Petri nets began to be exploited in the 1960s, many different types of models have been introduced and used. The most popular models are presented in this paper, their main advantages are shown and the dif-

ferences between them are mentioned. Everything is described according the teaching of formal methods used in digital systems design especially during the design of peripheral devices of computers, where some asynchronous and parallel actions without any coupling to internal clock frequency have to be designed and modeled.

This basic knowledge and method of the model construction is enlarged and exploited in student group projects. Petri net based models have been used e.g. in the design of a processor or a control system architecture with special properties, e.g. fault-tolerant or fault-secure, hardware-software co-design, computer networks architecture, etc. This has led to the development of PN models in

DOI: 10.4018/978-1-60566-774-4.ch008

some Petri net design tools and then the analysis and simulation of models using these tools. After this high-level design has been developed and validated it becomes possible, through automatic translation to a Hardware Description Language obviously used in digital hardware design (VHDL or Verilog design languages), to employ proper implementation in a programmable hardware (FPGA – field programmable gate array or CPLD – complex programmable logic device).

Our students have been teaching and making many experiments based on the massive using of FPGA or CPLD development kit. They have practical skills from the 3rd semester of bachelor studies (Kubátová, 2005; Bečvář, 2006). It enables a custom device to be rapidly prototyped and tested (however the ASIC implementation is also possible). An FPGA version of a digital circuit is likely to be slower than the equivalent ASIC version, due to the regularly structured FPGA wiring channels compared to the ASIC custom logic. However, the easier custom design changes, the possibility of easy FPGA reconfiguration, and relatively easy manipulation make FPGAs very good final implementation bases for our experiments. This is most important due to strict time schedule of these student group projects – everything must be finished during one semester.

Most models used in the hardware design process are equivalent to the Finite State Machine (FSM), (Adamski, 2001; Erhard, 2001; Gomes, 2001; Uzam, 2001). It is said that the resulting hardware must be deterministic, but we have found real models that are not equivalent to an FSM. Therefore we have concentrated on those models with really concurrent actions, with various types of dependencies (mutual exclusion, parallel, scheduled), and have studied their hardware implementation.

Petri nets are a good platform and tool in the “multiple-level” design process. They can serve as a specification language on all levels of specifications, and as a formal verification tool throughout these specification and architectural

description levels. The first problem to be solved during the design process is the construction of a good model, which will enable the specification and further handling and verification of the different levels of this design. Therefore this paper presents such model constructions on the basis of a number of simple examples. These experiments can use the automatic translation process from PNML language to the synthesized VHDL description that can be easily implemented in FPGA. We have used universal VHDL description divided into several blocks. The blocks can be easily modified.

The paper is organized as follows. The brief description of used hardware and software tools is in section 2. Section 3 contains the concrete example and construction of its models by Petri nets of several types. The brief description of experiments for the dining philosophers’ problem, the producer-consumer PN model and a railway critical rail are described in section 4. Section 5 concludes the paper.

TECHNOLOGY AND DESIGN TOOLS

Xilinx and Altera are two most significant companies in the market of programmable devices. Their products, including circuits, design kits and development systems, are comparable. As Xilinx provides better university support, we have decided to use Xilinx products. ISE 7.1i is the development system in which students design their circuits. Our students have practical skills with the design kits Digilent XCRP (Digilent, 2009), equipped with CPLD Xilinx CoolRunner XCR3064 (Xilinx, 2009) and FPGA Xilinx Spartan2E.

ModelSim simulator is used for simulation. In introductory and intermediate course students simulate designs created in Xilinx ISE. In advanced course designs are created in HDL Designer and then again simulated in ModelSim.

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