Chapter 6

Optimizing CMOS Inverter Characteristics With Evolutionary Algorithm Strategies

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ABSTRACT

This work uses the Dragonfly Algorithm (DA) and Drosophila Food Search Optimization (DFO) to enhance the switching characteristics of CMOS technology. Inspired by the food-search behavior of Drosophila Melanogaster and Dragonflies, both algorithms optimize single- and multi-objective problems and are compared with Whale Optimization Algorithm (WOA) and Particle Swarm Optimization (PSO). The study focuses on identifying optimal design variables for a CMOS inverter with symmetric switching. DA and DFO were further tested on a differential amplifier with a current mirror load, demonstrating their effectiveness in more complex circuits. The solutions were verified using SYNOPSYS HSPICE with UMC 180nm process technology, highlighting differences between algorithmic and simulation results. While all algorithms showed quick convergence, DA outperformed DFO and PSO in meeting design

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objectives, providing the most optimal solution for the circuit design.

1. INTRODUCTION

There are several current digital systems that don't work without a CMOS (Complementary Metal-Oxide-Semiconductor) inverter. CMOS technology is extensively used in digital circuits because of its minimal power usage, superior noise immunity, and straightforward integration. CMOS inverters are essential for the efficient operation of many digital systems (Sreenivasulu, 2022; Ortiz-Conde, 2022). The operational speed of a digital circuit system is essential for assessing its overall performance, efficiency, and success. It affects system responsiveness, data throughput, real-time processing, power efficiency, and market competitiveness. Accelerated systems not only enhance performance but also facilitate the development of more intricate applications, hence propelling innovation across several sectors (Xie, 2021; Pradhan, 2021). The processing speed of digital integrated circuits (ICs) is significantly affected by the switching attributes of the logic gates comprising these circuits. The characteristics include rising time (t_r), fall time (t_f), and propagation delays - namely, the high-to-low propagation delay (t_{pHL}) and low-to-high propagation delay (t_{pLH}). Rise time refers to the duration required for a signal to shift from a low voltage (which is frequently 10% of the end value) to a high voltage (usually 90% of the ending value). A reduced rise time indicates that the gate transitions from a low state to a high one more rapidly, enhancing the overall speed of the circuit. Fall time refers to the duration required for a signal to transition from a high voltage (which is usually 90% of the final value) to a low voltage (about 10% of the final value) (Ma et al., 2022). Analogous to rise time, reduced fall durations signify expedited transitions from a high condition to a low one. t_{pHL} is the duration required for a gate's output to shift from a high state to a low state after an input change. t_{pHL} is the duration required for a gate's output to shift from a high state to a low state after an input change. t_{pLH} is the duration required for a gate's output to shift from a low state to a high state after an input alteration (Sharma & Roy, 2021). So it's critical to optimize the switching characteristics from the beginning of the design process itself. According to this, transistor sizes (i.e. width (W) and length (L)) and other component values, such as load capacitance (C_L), which are design factors during the optimization process, have a direct impact on the switching characteristics (Ferrari et al., 2022).

The optimization of t_r, t_f, t_{pHL} and t_{pLH} is a cornerstone of efficient digital circuit design. These parameters collectively define the switching speed and reliability of digital circuits. By minimizing these values, designers can accelerate signal transitions within the circuit, leading to faster overall operation and improved performance. However, this optimization process is far from trivial, requiring meticulous planning and careful consideration of interrelated factors such as speed, power consumption, and signal integrity. In digital systems, faster switching speeds are synonymous with higher operational frequencies and improved data throughput (Kundu & Mandal, 2014). This makes the reduction of rise and fall times critical, as these parameters dictate how quickly a signal transitions between its logical states. Shorter rise and fall times enable faster toggling of digital gates, which directly enhances system performance. Similarly, minimizing propagation delays ensures that signals traverse through the circuit more quickly, reducing latency and improving responsiveness in real-time applications. While faster circuits are desirable, achieving this goal often involves trade-offs. For example, reducing rise and fall times typically requires larger transistors with higher drive strength, which can increase power consumption and contribute to heat dissipation. Conversely, optimizing propagation delays may necessitate changes to