Design of a Simple and Low-Cost Calculator in the Laboratory Using FPGA

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INTRODUCTION

It is a common practice to realize specific operations/algorithms in embedded systems using programmable general-purpose processors. However, an alternative solution to software implementation is the design of application specific dedicated hardware in order to achieve high performance system at relatively low cost. The advancement in VLSI technology makes it attractive for implementation in any application specific task to minimize the size and power requirements which in turn reduce the cost.

In this view, we aim to design a prototype of a simple, low cost calculator in the laboratory which would enable us to perform the basic arithmetic operations like addition, subtraction, multiplication, division along with some logical operations. Though a great amount of work had been done on Arithmetic and Logic Unit (ALU) design (O-Cisneros et al. 2005; William 2006; Xiao et al. 2008; Oztekin et al. 2011; Singh 2014), it is still a challenging task to implement the algorithms successfully in hardware. FPGAs are matrix of configurable logic blocks connected by programmable interconnects and are used to implement desired functionality after manufacturing (Brown et al. 1992; Rose et al. 1993). Due to the programmable nature of FPGAs, they are used in many application fields, such as ASIC prototyping, wireless communications, video/image processing, surveillance, industrial automation, information appliances, home networking & monitoring, residential set top boxes etc. Beside the promising computational platform of FPGAs, parallel nature of computing and overall non recurring costs make them significantly faster for some applications (Rose et al. 1993; Oldfield & Dorf 1995).

The objective of this work is to design an alternative, simple, low power, cost effective calculator in the laboratory. FPGA prototyping of this reusable, dynamic calculator is a reliable way to verify the design in hardware (Lysaght 1993; Oldfield & Dorf 1995; Kalte et al, 2002). Initial step of design is to frame out the simple arithmetic and logical operations and then it would be upgraded for scientific calculations (inclusion of trigonometric operations and logarithmic calculations). In this work, design guideline of simple arithmetic circuits such as adders, subtractors, multiplier, divider and some logical units are studied and assembled to configure the dynamic calculator. The inputs may be applied either

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by using switches in the FPGA board or a conventional PS/2 keyboard that is connected externally but interfaced to FPGA and the results are displayed on the (2 × 16) paneled LCD screen available on the FPGA board. The design algorithm of this operation is very simple and hardware resource requirement is also minimal. Hence any low-level FPGA hardware is sufficient to implement the design in the laboratory.

Background Architecture of FPGA

Since 1960, there have already been four generations of ICs .viz SSI (small scale integration), MSI (medium scale integration), LSI (large scale integration), and VLSI (very large scale integration). An electronic circuit usually consists of a CPU, ROM, RAM and other peripherals on one board. VLSI is a process of combining thousands of transistors into a single chip occupying a relatively smaller area (https://electronicsforu.com/resources/learn-electronics/vlsi-developments-ic-fabrication).

The primary advantages of using VLSI technology are:

- Reducing the size of circuits.
- Reducing the effective cost of the devices.
- Increasing the operating speed of circuits.
- Requirement of less power than discrete components.

Field Programmable Gate Arrays (FPGAs) are semiconductor devices that may be programmed according to specific tasks after manufacturing, while Application Specific Integrated Circuits (ASICs) are manufactured for specific design tasks. There are some specific software to configure FPGA as simple as an AND gate to as complex as the multi-processor (Zhu et al. 2009). The FPGA stores the specific configuration in RAM, which is why the configuration is lost when there is no power connectivity (Lysaght 1993; Oldfield & Dorf 1995). Hence, they must be configured every time the power is on. FPGAs are prefabricated on silicon chips that can be programmed electrically to implement the desired functions. As shown in Fig. 1, FPGA Architecture consists of three major components —

- Configurable Logic Blocks (CLB), which implement logic functions
- Programmable Routing (interconnects), which implements the functions
- I/O blocks, which are used to make off-chip connections

Configurable Logic Blocks: These blocks provide basic computation and storage elements used in digital systems. A basic logic element consists of programmable look-up-tables, a flip-flop, and some fast carry logic to reduce the area and delay cost.

Programmable Routing: The programmable routing establishes a connection between logic blocks and Input/Output blocks to complete a user-defined design unit. It consists of horizontal and vertical routing channels which again containing multiplexers, pass transistors and tri-state buffers. Pass transistors and multiplexers are used in a logic cluster to connect the logic elements.

Programmable I/O Blocks: The programmable I/O pads are used to interface the logic blocks and routing architecture to the external components. The I/O pads and the surrounding logic circuits form the I/O blocks.

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