Chapter 7
CNT as Interconnects

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ABSTRACT

The chapter will start with brief introduction to the interconnects and its importance in an integrated circuit at deep sub-micron technology nodes. The brief discussion about the concept of scaling, interconnects models, and material in use are presented. The limitations of conventional materials at scaled down technology nodes will be discussed next. The focus of the chapter is to present the electrical equivalent circuit model to estimate the impedance parameters of SWCNT bundle and MWCNT bundle as interconnects at different nano-scaled technology nodes for global level interconnect length. Using ESC model of SWCNT, MWCNT, and copper, the performance comparative analysis for delay and power delay product (PDP) will be presented for different interconnect lengths at nano-scaled technology nodes. Finally, the chapter summary and conclusion will be written at the end of the chapter.

1. INTRODUCTION

An integrated circuit is created by combining thousands of transistors or devices or modules onto a single chip. After the introduction of Very Large Scale Integration (VLSI) circuits in 1970s, numerous functions can be performed on single IC chips. The electronics industry has shown a phenomenal growth in recent years. The high computational speed and efficient processing power is the driving force for technology up gradations. The number of complex functions is increasing in small package, so there has been steady increase in the level of integration as well. The beauty of integrated circuit lies in the ultimate performance in all aspects like chip area, cost, speed and power of all interconnected modules. So, interconnect issues

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are very important at scaled technology nodes. If the technology somehow fails to have a good interconnect, then total performance of IC will degrade due to high parasitic resistance and capacitances leading to even higher delay than transistors or logic gates. (Bakoglu & Meindl, 1985; Steinhögl et al., 2005)

2. VLSI INTERCONNECTS

Interconnects are thin conducting paths used to establish the electrical links between two or more than two nodes of the electrical circuit within the Integrated Circuits (IC). Different conducting materials have been used as interconnects in ICs. In early days the aluminum was used as interconnect material but due to its large resistivity at micro-scaled technology nodes, the copper was used as alternative material for interconnects in IC design. As technology is scaled down to nanometer technologies, the resistance of copper interconnects increased rapidly due to its small mean free path (MFP) (Kaushik & Majumder, 2015; Gholipour & Masoumi, 2012; Naeemi & Meindl, 2009; Srivastava et al., 2009; Burke, 2002). MFP of electrons is due to the combined effects of scattering (grain boundary and surface) and electromigration. Due to these disadvantages of copper as interconnect material at advanced technologies, the conventional copper material is replaced by other new materials. As the technology nodes are scaled down, the density of the devices is increasing and long interconnect lengths are required to interface all the devices. Therefore, the performance of an IC is mainly on basis of current carrying capacity and parasitic such as resistance, inductance and capacitance of the interconnect material (Das, Majumder, & Kaushik, 2014; Singh & Raj, 2015; Sandha & Sharma, 2018; Hosseini & Shabro, 2010; Pop et al., 2007). As technology nodes are scaled down, the device dimensions and supply voltages of ICs are also scaled down, the interconnect dimensions are also required to be scaled down to synchronized the dimensions (Singh & Raj, 2015). With advancement of technology nodes, more functions are to be incorporated in VLSI chips. Therefore, the required interconnects length is exponentially increasing to connect millions of active devices in with in an IC. The basic structure of Driver Interconnects Load (D-I-L) is shown in Figure 1.

In DIL, a CMOS based inverter is used to drive interconnect with a capacitive load as shown in Figure 1. To evaluate the performance of interconnect, the equivalent parameters of used material will be used as R-L-C circuits model. These impedance parameters of interconnects are depending on the technology dependent cross-sectional dimensions and properties of the material used as interconnects. (Steinhögl et al., 2005; Majumder, Kaushik & Manhas, 2014)