Chapter 4
CNTFET for Logic Gates Design

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ABSTRACT

The novel characteristics of CNTFET have eliminated many technological and fundamental hindrances being faced by CMOS transistors. CNTFET is emerging as prospective replacement for CMOS transistors in digital circuits and systems. This chapter introduces design of CNTFET-based basic logic gates. The basic logic gates analyzed are inverter, NAND, and NOR gates. The designed gates are evaluated in terms of delay, power consumption, and figure-of-merit power-delay-product (PDP). The standard H-SPICE CNTFET model of Stanford University has been used for all simulations. The impact of dielectric material variations on performance parameters of carbon nanotube field effect transistor based universal gates has been analyzed. Comparison between CMOS and CNTFET-based logic circuits is carried out for different dielectric material at 16 nm technology node.

1.1 INTRODUCTION

Carbon Nanotube Field Effect Transistor (CNTFET) make use of carbon nanotubes (CNTs) as channel material while a traditional MOSFET uses bulk silicon as a channel material (Appenzeller, Lin, Knoch, Chen, & Avouris, 2005). It was first

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experimentally testified in 1998, since then there is a continuous development in CNTFETs. If standard bulk silicon thickness is 0.5mm then from that prospective only 5-10 nm of area on the top surface level is being used for transistor action. For *n*-type or *p*-type CNTFETs, highly doped source and drain terminals are formed, for *n*-type group 5 elements such as phosphorus, arsenic and for p-type group 3 elements such as boron, gallium are used. CNT act as a channel. It is hollow inside with gate-all-around structure. It is used to mitigate short channel effect. Instead of using bunch of CNTs, SWCNT can be used to achieve area efficiency and low power consumption device. Placing of carbon nanotubes inside the trenches between source and drain is a difficult process. CNT conductivity depends upon its chirality; it can be semiconducting, metallic or semi-metallic in nature. 1-D structure of CNT makes scattering rare, which give rise to ballistic transport. CNT can operate at elevated temperature (~250°C), very high current carrying capability (~ 1010 A/ cm^2), larger mean free path etc. (Hoenlein, Kreupl, Duesberg, Graham, Liebau, Seidel & Unger, 2003). With the use of CNTs in FET high performance, high impedance, faster switching speed can be achieved. CNTFET structure with CNTs as a channel between source and drain terminal is shown in Figure 1.

Due to these remarkable advantages offered by CNTFETs, lot of research has been going on modeling and making its way towards digital circuits and systems to compute its performance (Raychowdhury, Mukhopadhyay, & Roy, 2004). CNTFET is one of the best promising technologies to substitute existing silicon technology because of following reasons:

1. The working principle and device structure is almost same as basic MOSFET device.
2. CNTFETs have excellent current carrying capability.
3. CNTs are light in weight and work on the principle of ballistic transport.
4. CNTFETs have sharp sub-threshold slope.
5. Improved current density (CNTs has current density nearly three times higher than that of silicon device).
6. Electron mobility will be high due to non-equilibrium transport mechanism.
7. High drive current.
8. No degradation down to 9 nm channel length.

Basically digital system design is associated with the binary logic based on two valued logic (‘0’ or ‘1’) in Boolean space (Murotiya, Gupta, & Pandit, 2014; Lin, Kim, & Lombardi, 2011). Basic gate inverter and universal gates such as NAND and NOR gate forms the basics of any digital circuitry. Hence the optimum design of universal gates in terms of low power, lower delay, and good figure-of-merit (FOM) is desired for overall performance of digital circuit /system. Nowadays, speed and