Chapter XVI

Reconfigurable Embedded Medical Systems

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ABSTRACT

This chapter introduces reconfigurable design techniques for light-weight medical systems. The research presented in this chapter demonstrates how the wise use of reconfiguration in small embedded systems is an approach that is beneficial in heterogeneous medical systems. By shrewdly designing embedded systems, one can make efficient use of limited resources through efficient and effective reconfiguration schemes that balance the tradeoffs between power consumption, memory consumption, and interoperability in heterogeneous environments. Furthermore, several reconfigurable architectures and algorithms presented in this chapter will assist researchers in designing efficient embedded systems that can be reconfigured after deployment, which is an essential feature in embedded medical systems.

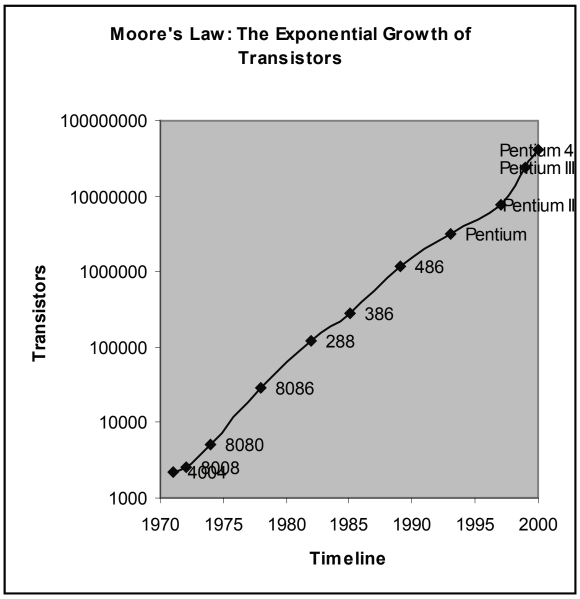
INTRODUCTION

Moore's Law has allowed processor performance to double approximately every 18 months due to continuous breakthroughs in transistor technology. Although processor performance is paramount to high-performance computing, the world of embedded systems has other priorities: namely the minimization of power and silicon area. Moreover, embedded systems are specialized systems that often communicate via wireless networks with limited bandwidth and have limited communication and memory resources. The shrewd design of embedded systems, however, can make efficient use of limited resources through efficient reconfiguration schemes that balance the tradeoffs between power consumption, memory consumption, and interoperability in heterogeneous environments. Several of these projects are discussed here in the context of a reconfigurable fabric—literally, a wearable motherboard—as well as several customizable medical devices. Adaptive algorithms for communication throttling in response to dynamic environmental changes are also described. Lastly, we highlight the need to reprogram embedded systems following an extended period of time already employed in their respective environments. The architectures and algorithms presented demonstrate how well designed embedded systems can benefit from reconfigurability.

Moore's Law

In 1965 Gordon E. Moore, then R&D director at Fairchild Semiconductor, quantified the astounding growth of the new technology of semiconductors. Moore predicted that manufacturers would double the density of components per integrated circuit at approximately regular intervals (18 months), and would continue to do so until the molecular limits of silicon technology could be reached. This prediction—*Moore's Law*—has held steady for the past 40 years, although the semiconductor industry is beginning to reach the limits of what is physically achievable with silicon. Moore's Law, as applied to various processor families introduced by Intel (Schaller, 1999) is shown in Figure 1.

Figure 1. Number of transistors in Intel microprocessors almost has been doubled every two years.



Until the past decade, circuit designers were afforded the luxury of neglecting the electrical performs of wires and metal interconnections beyond a cursory accounting of their parasitic capacitance. Effectively, they were able to increase transistor channel width to provide larger drive currents, thereby increasing transistor-level circuit performance. Unfortunately, transistors have shrunk to a point where interconnect latency and energy dissipation dominate overall transistor performance. On the other hand, wire and interconnect size is shrinking, effectively reaching its physical limit. Clearly, a wire cannot be narrower than an electron; and due to the effects of electro-migration, a significant number of electrons are dissipated during basic microelectronic communication. In short, the physical

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