

Chapter 11

FPGA–Based Re–Configurable Architecture for Window–Based Image Processing

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ABSTRACT

In this proposed book chapter, a simple but efficient presentation of Median Filter, Switching Median Filter, Adaptive Median Filter and Decision-Based Adaptive Filtering Method and their hardware architecture for FPGA is described for removal of up to 99% impulse noise from Digital Images. For hardware architecture, simulation is done using Xilinx ISE 14.5 software of XILINX. For implementation, these approaches utilize Genesys VIRTEX V FPGA device of XC5VLX50T device family. In this approach, we proposed an efficient design for suppression of impulse noise from digital images corrupted by up to 99% impulse noise using decision based adaptive filtering method as well as preserve the details of image. The method works in two different stages – noise detection using switching technique and finally noise suppression and restoration. Experimental results show that our method perform better in terms of PSNR below 80% noise density but above 80% noise density it is almost comparable with the latest methods.

1. INTRODUCTION

Now a day, in image processing, Filtering is a basic need because of different kinds of noise invoke into an image. Noise is any kind of unwanted signal. For our design the authors consider the impulse noise which is also known as classical salt and pepper noise for gray-scale image. Impulse noise exists in many practical applications and can be generated by various sources, including many man-made phenomena

DOI: 10.4018/978-1-5225-5204-8.ch011

such as unprotected switches, industrial machines, and car ignition systems. Images are often corrupted by impulse noise due to a noisy sensor or channel transmission errors. Impulse noise can appear because of a random bit error on a communication channel. The most common method used for impulse noise suppression for gray-scale and colour images is the median filter. In the area of image processing two important applications are needed that is noise filtering and image enhancement (Gonzalez & Woods, 2009). Many types of noises including impulse noises are the normal sources of image corruption which are the subset of digital signals (Gonzalez & Woods, 2009). Noise filtering aim is to eliminate noise by affecting lesser on the original images (Andreadisand & Louverdis, 2004). Very high contrast to the surrounding of impulse noise comprises a set of random pixels (Petrou & Bosdogianni, 2000; Wang & Lin, 1997). Some common causes for impulse noise are transmission of image in noisy channel, camera sensors containing malfunctioned pixels, or faulty memory locations in hardware (Chan, Ho, & Nikolova, 2005). Filters are chosen according to their noise pattern in the field of image processing. Comparing with linear filters, nonlinear filters give better results in case of order statistics filters. A proposal was made for correlation between a number of nonlinear filters and vectors by using various distance measurement (Arce et. al., 1986, Pitas et. al., 1990 and Hodgson et. al., 1985). Analysis and comparisons of different filtering algorithms are already discussed in quite a few literatures and number of different improved algorithms are put forwarded (Chang, 1995; Ng et. al., 2006). The computational complexity for filtering applications wants an amount of huge data for presenting image information in a digital way. Comparing with software implementation, hardware implementation can result better speed with the help of pipelining and parallelism technique. Semi-custom hardware device i.e., Field programmable gate arrays (FPGAs) achieve advantage over Application specific integrated circuits (ASIC) and Digital signal processors (DSPs). Reconfigurable nature of FPGAs consisting with pipeline and parallelism technique make it efficient to reduce the complexity of algorithms and simplify the debugging and verification. In this report, the algorithms of median and switching median filter are proposed in the means of software as well as hardware implementation for removal of impulse noise considering salt and pepper noise from gray scale images. Utilization of median filter and switching median filter is done in such a way that experimental results show their improved performances. The proposed algorithms are capable for 8-bit gray scale image processing and as image neighbourhood, 3x3 and 5x5 moving window are chosen which are also expandable as the design needs. The hardware implementations are done on FPGAs which associate with flexibility, high performance and low cost (Pratt, 1991). The software implementation for proposed algorithms is done on MATLAB (v 2012a). The software design, compilation and simulation are associated with that. The hardware structure is designed and simulated using System Generator of Xilinx ISE (14.5) developed by XILINX. The system level simulations are done on Matlab and System Generator and RTL level simulations are done on Isim Simulator. The proposed designs are realized on Genesys Virtex V FPGA Board of XC5VLX50T device family. These two designs can be implemented for real time imaging applications where ultimate importance is fast processing (Dougherty & Laplante, 1995). This paper is organized with some stages. At first stage, a brief overview of median and switching median filter is provided, in next stage the algorithms are provided, after that the architectures with their functional stages are presented in detail. In the next stage performances of software and hardware implementation are provided following the timing, area and power analysis. In the last stage conclusions are discussed in detail. Now, the discussions are based on a new technique for removing high density impulse noise from a corrupted image without changing the image details. Removal of impulse noise from highly corrupted images is important for different kind of imaging applications i.e. image segmentation, edge detection and image compression (Nooshyar, 2013). In signal processing noise suppression and

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