Chapter 1
Power Optimization Using Clock Gating and Power Gating: A Review

Arsalan Shahid
HITEC University, Pakistan

Muhammad Yasir Qadri
University of Essex, UK

Saad Arif
HITEC University, Pakistan

Saba Munawar
COMSATS Institute of Information Technology, Pakistan

ABSTRACT

The scaling of CMOS technology has continued due to ever increasing demand of greater performance with low power consumption. This demand has grown further by the portable and battery operated devices market. To meet the challenge of greater energy efficiency and performance, a number of power optimization techniques at processor and system components level are proposed by the research community such as clock gating, operand isolation, memory splitting, power gating, dynamic voltage and frequency scaling, etc. This chapter reviews advancements in the dynamic power optimization techniques like clock gating and power gating. This chapter also reviews some architectures and optimization techniques that have been developed for greater power reduction without any significant performance degradation or area cost.

INTRODUCTION

Recent advances in the field of computer architecture have marked power consumption as one of the major design constraints (Farkas, Jouppi, Ranganathan, & Tullsen, 2015). Power optimization is now a prerequisite for not only portable and mobile computing systems but also for advanced multicore platforms (Hager, Treibig, Habich, & Wellein, 2014). An energy-efficient design strives to deliver optimum throughput while minimizing power consumption (Hanumaiah & Vrudhula, 2014). Current research on energy-efficient processor architectures targets various abstraction levels, spanning from integration technology to algorithmic optimization. Integrated Chip (IC) manufacturing technologies

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have largely improved during the past decades to cater the greater performance demands, while being energy efficient. Modern multiprocessor systems have billions of transistors with operating frequencies in gigahertz (GHz) range (Daud, Ahmad, & Lynn, 2014). Power optimization in such highly integrated systems is not just an option but a basic requirement. A microprocessor experiences both static and dynamic power consumption; the static power is mainly contributed by leakage current in the device, whereas the dynamic power consumption is a function of toggling frequency. A number of techniques have been developed to control the dynamic power of **C**omplementary **M**etal-**O**xide **S**emiconductor (CMOS) circuits in general, and processors in particular such as clock gating (CG), pre-computation, operand isolation, memory splitting, power gating, body biasing, dynamic voltage-frequency scaling, etc. (Arora et al., 2014; Shah & Ahir, 2013).

This chapter introduces and reviews recent advancements in *clock gating (CG)* and *power gating* (PG) techniques in details. The rest of this chapter is organized as follows: the next section presents a background of power optimization techniques and motivation to use clock gating and power gating among them. Then, a detailed review of clock gating techniques is presented in the next section. After that, power gating techniques to optimize power consumption in a microprocessor are described. Finally, the chapter concludes.

BACKGROUND

Reducing the power consumption has become one of very important research interest and a great challenge in various computing platform for the past decade. In this section we will discuss various techniques used for power optimization. Moreover, we will discuss the advantages of power gating and clock gating techniques over the other available techniques.

Power dissipation has emerged as an important factor in the design phase of a microprocessor. Careful and intelligent design is required at different levels of computer system to obtain optimal power performance. Therefore, it is very important to know the sources of energy consumption at different levels of memory hierarchies. Various energy models have been presented to understand the accurate power consumptions by integration with different cycle accurate simulators. One such example is energy models of multilevel cache memory presented by Qadri et al. (Qadri, M. Y., & McDonald-Maier, K. D., 2010). Energy models can also be subdivided in to three types, i.e., CPU level Energy models (Brooks, D. M. et al, 2000), complete system level models and interconnect level energy models. Hence, energy models do provide a very deep level of energy consumption analysis and result in to power optimization. Then comes the Dynamic Power Measurement (DPM) techniques, which can be classified into three subcategories:

1. CPU level DPM,
2. Complete system level DPM, and
3. Parallel system-level DPM.

These techniques target energy consumption reduction at run-time by selectively turning off or slowing down components when the systems are idle or serving light. DPM techniques can be applied in different ways and are applied at different levels; in accordance to which they lie in the three mentioned categories e.g. dynamic voltage scaling changes the processor's supply voltage and similarly frequency