

# Reconfigurable Computing Technologies Overview

R

**Kai-Jung Shih***National Chung Cheng University, ROC***Pao-Ann Hsiung***National Chung Cheng University, ROC*

## INTRODUCTION

Reconfigurable computing is breaking down the barrier between hardware and software design technologies. The segregation between the two has become more and more fuzzy because reconfigurable computing has now made it possible for hardware to be programmed and software to be synthesized. Reconfigurable computing can also be viewed as a trade-off between general-purpose computing and application specific design. Given the architecture and design flexibility, reconfigurable computing has catalyzed the progress in hardware-software codesign technology and a vast number of application areas such as scientific computing, biological computing, artificial intelligence, signal processing, security computing, and control-oriented design, to name a few.

In this article, we briefly introduce why and what is reconfigurable computing in the introduction section. Then, the resulting enhancements of hardware-software codesign methods and the techniques, tools, platforms, design and verification methodologies of reconfigurable computing will be introduced in the background section. Furthermore, we will introduce and compare some reconfigurable computing architectures. Finally, the future trends and conclusions will also be given. This article is aimed at widespread audiences, including both a person not particularly well grounded in computer architecture and a technical person.

## Why Reconfigurable Computing?

With the popularization of the use of computers, computer-aided computing can be roughly divided into two technical areas, one of which is general-purpose computing and the other is application-specific integrated circuit (ASIC) computing.

On one extreme, general-purpose computing was accomplished by the world's first fully operational electronic general-purpose computer, called *Electronic Numerical Integrator and Calculator* (ENIAC), built by J. Presper Eckert and John Mauchly. But it is well-known as *von Neumann computer* because ENIAC was improved by

John von Neumann (Hennessy & Patterson, 2007). A general-purpose computer is a single common piece of silicon, called a *microprocessor*, that could be programmed to solve any computing task. This means many applications could share commodity economics for the production of a single integrated circuit (IC). This computing architecture has the flexibility and superiority that the original builders of the IC never conceived (Tanner Research, 2007).

On the other extreme, an ASIC is an IC specifically designed to provide unique functions. ASIC chips can replace general-purpose commercial logic chips, and integrate several functions or logic control blocks into one single chip, lowering manufacturing cost and simplifying circuit board design. Although the ASIC has the high performance and low power advantages, its fixed resource and algorithm architecture result in drawbacks such as high cost and poor flexibility.

As a tradeoff between the two extreme characteristics, reconfigurable computing has combined the advantages of both general-purpose computing and ASIC computing. A comparison among the different architecture characteristics is illustrated in Table 1 (Tredennick, 1996; Tessier & Burleson, 2001).

From Table 1, we observe that reconfigurable computing has the advantage of programmable or configurable computing resources, called *configware* (TU Kaiserslautern, 2007a), as well as configurable algorithms, called *flowware* (Hartenstein, 2006; TU Kaiserslautern, 2007b). Further, the performance of reconfigurable systems is better than general-purpose systems and the cost is smaller than that of ASICs. The main advantage of reconfigurable system is its high flexibility, while its main disadvantage is its high power consumption. The design effort in terms of nonrecurring engineering (NRE) cost is between that of general-purpose processor and ASICs.

Because reconfigurations of underlying resources help achieve the goals of balance among performance, cost, power, flexibility, and design effort. The reconfigurable computing architecture has enhanced the performances of large variety of applications, including embedded systems, SoCs, digital signal processing, image processing, network

Table 1. Comparison of representative computing architecture

| Computing Architecture | Programming source |            | Advantage   |        |        |             |                     |
|------------------------|--------------------|------------|-------------|--------|--------|-------------|---------------------|
|                        | Resources          | Algorithms | Performance | Cost   | Power  | Flexibility | Design effort (NRE) |
| General-purpose        | Fixed              | Software   | Low         | Low    | Medium | High        | Low                 |
| ASIC                   | Fixed              | Fixed      | High        | High   | Low    | Low         | High                |
| Reconfigurable         | Configware         | Flowware   | Medium      | Medium | High   | High        | Medium              |

security, bioinformatics, supercomputing, boolean SATisfiability (SAT), spacecrafts, and military applications. We can say that reconfigurable computing will widely, pervasively, and gradually impact human lives.

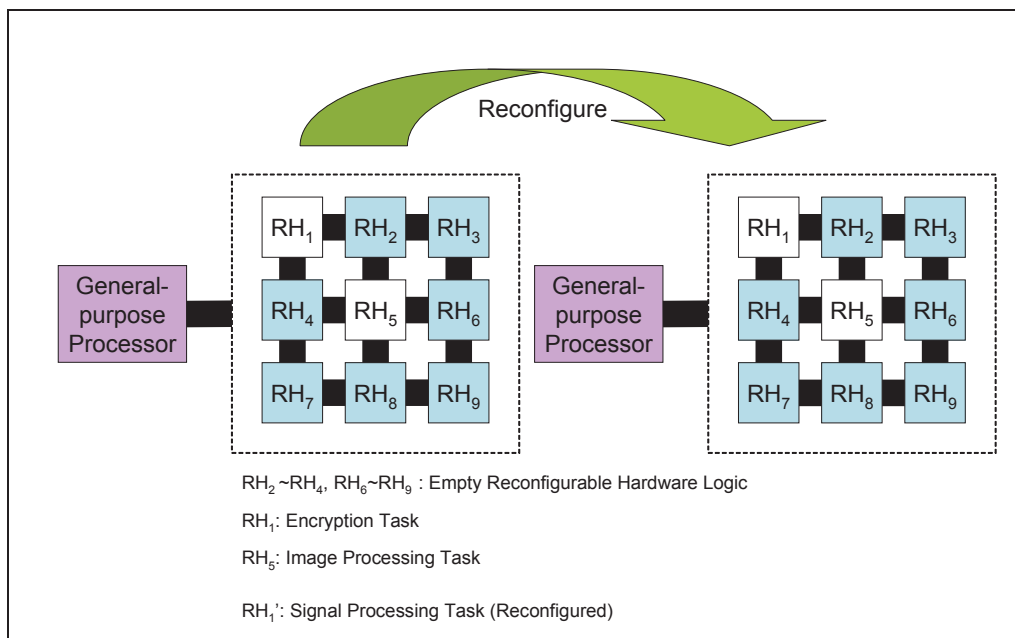
## What is Reconfigurable Computing?

In 1960, Estrin (1960) first proposed the term “reconfigurable computing.” The reconfigurable computing architecture is composed of a general-purpose processor and reconfigurable

hardware logic. The reconfigurable computing architecture can be concisely defined as *Hardware-On-Demand*<sup>TM</sup> (Schewel, 1998), *general purpose custom hardware* (Goldstein et al., 2000) or a *hybrid approach between ASICs and general-purpose processors* (Singh et al. 2000).

We illustrate a general reconfigurable computing architecture in Figure 1. In this architecture, the reconfigurable hardware logic executes application-specific computation intensive task, such as encryption ( $RH_1$ ) and image processing ( $RH_5$ ) as shown in Figure 1. The processor is used to

Figure 1. Reconfigurable computing



8 more pages are available in the full version of this document, which may be purchased using the "Add to Cart" button on the publisher's webpage: [www.igi-global.com/chapter/reconfigurable-computing-technologies-overview/14055](http://www.igi-global.com/chapter/reconfigurable-computing-technologies-overview/14055)

## Related Content

---

### Analysis and Comparison of Neural Network Models for Software Development Effort Estimation

Kamlesh Dutta, Varun Gupta and Vachik S. Dave (2019). *Journal of Cases on Information Technology* (pp. 88-112).

[www.irma-international.org/article/analysis-and-comparison-of-neural-network-models-for-software-development-effort-estimation/223177](http://www.irma-international.org/article/analysis-and-comparison-of-neural-network-models-for-software-development-effort-estimation/223177)

### What Drives Malaysian E-Government Adoption?: An Empirical Analysis

Alain Yee-Loong Chong (2013). *Managing Information Resources and Technology: Emerging Applications and Theories* (pp. 80-90).

[www.irma-international.org/chapter/drives-malaysian-government-adoption/74501](http://www.irma-international.org/chapter/drives-malaysian-government-adoption/74501)

### Strategic Planning for Information Resources: The Evolution of Concepts and Practice

William R. King (1988). *Information Resources Management Journal* (pp. 1-9).

[www.irma-international.org/article/strategic-planning-information-resources/50903](http://www.irma-international.org/article/strategic-planning-information-resources/50903)

### Optimization of Favourable Test Path Sequences Using Bio-Inspired Natural River System Algorithm

Nisha Rathee and Rajender Singh Chhillar (2021). *Journal of Information Technology Research* (pp. 85-105).

[www.irma-international.org/article/optimization-of-favourable-test-path-sequences-using-bio-inspired-natural-river-system-algorithm/274280](http://www.irma-international.org/article/optimization-of-favourable-test-path-sequences-using-bio-inspired-natural-river-system-algorithm/274280)

### A Comprehensive Model for Assessing the Quality and Productivity of the Information Systems Function: Toward a Theory for Information Systems Assessment

Barry L. Myers, Leon A. Kappelman and Victor R. Prybutok (1997). *Information Resources Management Journal* (pp. 6-26).

[www.irma-international.org/article/comprehensive-model-assessing-quality-productivity/51030](http://www.irma-international.org/article/comprehensive-model-assessing-quality-productivity/51030)