Chapter 21
Simulations and Modeling of TFET for Low Power Design

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ABSTRACT

In Complementary Metal-Oxide-Semiconductor (CMOS) technology, scaling has been a main key for continuous progress in silicon-based semiconductor industry over the past four decades. However, as the technology advancement on nanometer scale regime for the purpose of building ultra-high density integrated electronic computers and extending performance, CMOS devices are facing fundamental problems such as increased leakage currents, large process parameter variations, short channel effects, increase in manufacturing cost, etc. The new technology must be energy efficient, dense, and enable more device function per unit area and time. There are many novel nanoscale semiconductor devices, this book chapter introduces and summarizes progress in the development of the Tunnel Field-Effect Transistors (TFETs) for low power design. Tunnel FETs are interesting devices for ultra-low power applications due to their steep sub-threshold swing (SS) and very low OFF-current. Tunnel FETs avoid the limit 60mv/decade by using quantum-mechanical Band-to-Band Tunneling (BTBT).

INTRODUCTION

With the continued miniaturization of MOSFETs, the OFF-state leakage current (I_{OFF}) is exponentially increasing with reduction of the threshold voltage imposed by the fundamental limit to 60 mV/decade subthreshold swing at room temperature (Singh, Ramakrishnan, Mookerjea, Datta, Vijaykrishnan, & Pradhan, 2010). This limits the on current (I_{ON}) and the I_{ON}-I_{OFF} ratio severely as the supply voltage is reduced. To overcome these problems, new engineering solutions like improving the structure of the device, considering different materials with various features (Si, SiGe, Ge, etc) in the channel region and new dielectric (high-k) are suggested which are being used for a better exploitation of these devices (Kamali, Moghaddam, & Hosseini, 2012). In recent years, there are many novel nanoscale semiconduc-

DOI: 10.4018/978-1-4666-8823-0.ch021

tor devices such as DG MOSFET, FinFET, Gate-All-Around (GAA), Tunnel FET etc. studied to obtain a minimum I_{OFF} and a maximum ratio of I_{ON}/I_{OFF} as well as high ON current to avoid these limitations.

Tunnel FETs (TFETs) are today being intensively investigated (Zhang, Zhao, & Seabaugh, 2006) as some of the most promising devices that would allow logic circuit operation voltages below 0.5 V and reduced static power consumption. These features are conceivable owing to the possibility of achieving sub-threshold switching slopes (<60 mV/decade) at room temperature, due to Band-To-Band Tunneling (BTBT) in gated reverse-biased p–i–n junctions (Choi, Park, Lee, & Liu, 2007). Transistors which use BTBT to inject carriers into the channel instead of injecting carriers over a barrier are not limited by 60 mV/decade turn-off (Kim, Kam, Hu, & Liu, 2009). These tunneling transistors (TFETs) are therefore of great interest for high I_{ON}/I_{OFF} at low voltages. TFET performance is limited by the BTBT generation rate which is exponentially dependent on the effective tunneling bandgap as well as effective carrier mass of the semiconductor (Sze & Ng, 2007). The obvious means to enhance TFET performance and scale V_{DD} is by scaling this effective tunneling bandgap. This can be achieved by moving from Si to Ge to even lower bandgap III-V materials (Ionescu, Boucart, Moselund, Pott, & Tsamados, 2007). Since low I_{OFF}keeps the standby power consumption low, a TFET with lowest $I_{OFF}$and largest I_{ON}/I_{OFF}at a reduced V_{DD} is desired for ultra-low voltage operation. Among the most studied and optimized TFETs architectures, thin film Double-Gated (DG) lateral p–i–n TFET (Boucart & Ionescu, 2007) and a p-i-n TFET with a delta-doped n+ at the source side are shown to offer remarkable for obtained high I_{ON}/I_{OFF} ratio and good output characteristics. (Kamali, Moghaddam, & Hosseini, 2012), (Krishnamohan, Kim, Raghunathan, & Saraswat, 2008).

The origins of the nanoscale semiconductor device i:e TFET and Impact-Ionization Metal–Oxide–Semiconductor (IMOS) transistors (Ionescu, Boucart, Moselund, Pott, & Tsamados, 2007) have been analyzed as candidates for future small slope electronic switches. It has been demonstrated that can offer significant power savings, especially in the standby mode. These new categories of switches have applications for ultra-low power logic and/or as power gating devices for future power management. The lower subthreshold swing can also achieved by using the recently proposed negative-capacitance FET (NC-FET) (Salahuddin, & Datta, 2008). or micro or nano-electromechanical (M/NEM) movable electrodes in M/NEM-FET or NEM relay devices (Abele, Fritschi, Boucart, Casset, 2005) in which the instability points between the electrical and the mechanical force are used to define super-abrupt transitions between the off and on states. Experimentally, an SS of less than 2mV per decade has been demonstrated, but electromechanical devices have their own limitations, such as voltage-scaling limitations, reliability issues and a stringent need for a controlled environment for robust operation. Since TFETs offer the potential for a low off current and a small SS, but they generally have a lower on current than conventional MOSFETs, so a smart design strategy could achieve a small SS average and a high I_{ON} without degrading I_{OFF}. So that, major technology boosters for all-silicon TFETs include (Boucart, Ionescu, & Riess, 2009), (Boucart, Riess, & Ionescu, 2009) the use of a high-κ gate dielectric, a more abrupt doping profile at the tunnel junction, a thinner body, higher source doping, a double gate, a gate oxide aligned with the intrinsic region, and a shorter intrinsic region and gate length. In addition, TFETs retain their excellent switching characteristics even at high temperature (Born, Bhuwalka, Schindler, Schindler, Abelein, Schmidt, Sulima, & Eisele, 2006) because the tunneling mechanism makes them almost insensitive to temperature changes. TFETs offer a solution for critical leakage power savings in Static Random Access Memory (SRAM). Six-transistor (6T) (Singh, Ramakrishnan, Mookerjea, Datta, Vijaykrishnan, & Pradhan, 2010) and 4T (Saripalli, Mohata, Mookerjea, Datta, & Narayanan, 2010) SRAM cell designs with CMOS and TFET technologies have been compared in terms of layout,