Chapter 5
Design of a Power Aware Systolic Array based Support Vector Machine Classifier

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ABSTRACT

This chapter presents a method for generating binary and multiclass Support Vector Machine (SVM) classifier with multiplierless kernel function. This design provides reduced power, area and reduced cost due to the use of multiplierless kernel operation. Binary SVM classifier classifies two groups of linearly or nonlinearly separable data while the multiclass classification provides classification of three non-linearly separable data. Here, at first SVM classifier is trained for different classification problems and then the extracted training parameters are used in the testing phase of the same. The dataflow from all the processing elements (PEs) are parallely supported by systolic array. This systolic array architecture provides faster processing of the whole system design.

INTRODUCTION

Methods for efficiently classifying two or more groups of data are the area of interest for many researchers and scholars. Till date various solutions to classification problem have been proposed to classify two or more groups of data, each method carrying their own efficiency and deficiency. One of the significant methods was introduced in 1936 by R.A. Fisher which is a simple method to classify two or more groups of data known as Linear Discriminant Analysis (LDA). The main reason to choose LDA could be its Analytical and computational simplicity and low error rates. But there is a lack of a variety of

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measurable continuous variables for relatively large data samples. This reduces the popularity of LDA. Another most significant method for classification was introduced in 1943 by Warren McCulloch and Walter Pitts was Artificial Neural Network (ANN). Because of its nature that a user can easily train the network with any dynamic and nonlinear examples and can classify any sets of data even without personal knowledge about the behavior of solved problem, it was quite popular during the period 1940-1990 before SVM was introduced. The newest classification method proposed is SVM which was introduced by Cortes and Vapnik in 1992. It is based on the concept of decision planes (Li, Zhu & Ogihara, 2006). This plane provides decision boundaries that help to discriminate classes with higher accuracies than the other known statistical classifier (Li, Zhu & Ogihara, 2006), (Preman & Suwapura, 1991). Though most SVM implementation based on software provides acceptable margins of accuracy, real time performance of such classifiers has always been an area of concern. Yet SVM classifiers have been preferred. This is because of the fact that unlike ANN, SVMs do not suffer from multiple local minima problems. Further, SVMs provide solutions to classification problems which are global and unique. Also, SVMs provide simple geometric implementation to class discriminations and provide sparse solution (Li, Zhu & Ogihara, 2006), (Preman & Suwapura, 1991). Moreover, unlike ANNs, SVMs have a computational complexity that doesn't depend upon the curse of dimensionality. ANNs are based on empirical risk minimization, while SVMs depend on structural risk minimization (Preman & Suwapura, 1991). As reported by open literature, existing general-purpose SVM architectures do not scale well in terms of required hardware resources, complexity, data transfer (wiring) and memory management. This is primarily because of two important constraints. First, the number of support vectors (SVs) and next, their dimensionality. An SVM with a small number of SVs, requires only a few computational modules. But several applications require a large number of high dimensional SVs.

The key consideration involved is related to reduction of the power requirement of the processor. Power reduction has become a crucial factor now days. Because as the power decreases, battery life as well as the life of whole hardware design increases. The vector product for the kernel module SVM consumes most of the time. This work presents a method for generating binary and multiclass SVM classifier with multiplierless kernel function. This design provides reduced power, area and reduced cost due to the use of multiplierless kernel operation. Binary SVM classifier classifies two groups of linearly or nonlinearly separable data while the multiclass classification provides classification of three linearly or nonlinearly separable data. Here, at first SVM classifier is trained for different classification problems and then the extracted training parameters are used in the testing phase of the same. The dataflow from all the processing elements (PEs) is parallely supported by systolic array. This systolic array architecture provides faster processing of the whole system design.

BACKGROUND

In the field of image processing, computer vision, bio-informatics, classification of data is an area of study for many researchers and scholars from the beginning. SVMs are dynamic and powerful learning methods which provide excellent generalization performance for a wide range of regression and classification problem. Previous software implementations of SVM have reported high classification accuracy. But software designs can't meet the real time requirements because these designs can't take the advantage of parallelism inherent in the SVM algorithm. Thus, the hardware implementation of SVM can increase total simulation time and synthesis time.