Chapter 5
Vulnerabilities of Secure and Reliable Low-Power Embedded Systems and Their Analysis Methods: A Comprehensive Study

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ABSTRACT

Due to the increase in popularity of mobile devices, it has become necessary to develop a low-power design methodology in order to build complex embedded systems with the ability to minimize power usage. In order to fulfill power constraints and security constraints if personal data is involved, test and verification of a design's functionality are imperative tasks during a product's development process. Currently, in the field of secure and reliable low-power embedded systems, issues such as peak power consumption, supply voltage variations, and fault attacks are the most troublesome. This chapter presents a comprehensive study over design analysis methodologies that have been presented in recent years in literature. During a long-lasting and successful cooperation between industry and academia, several of these techniques have been evaluated, and the identified sensitivities of embedded systems are presented. This includes a wide range of problem groups, from power and supply-related issues to operational faults caused by attacks as well as reliability topics.

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INTRODUCTION

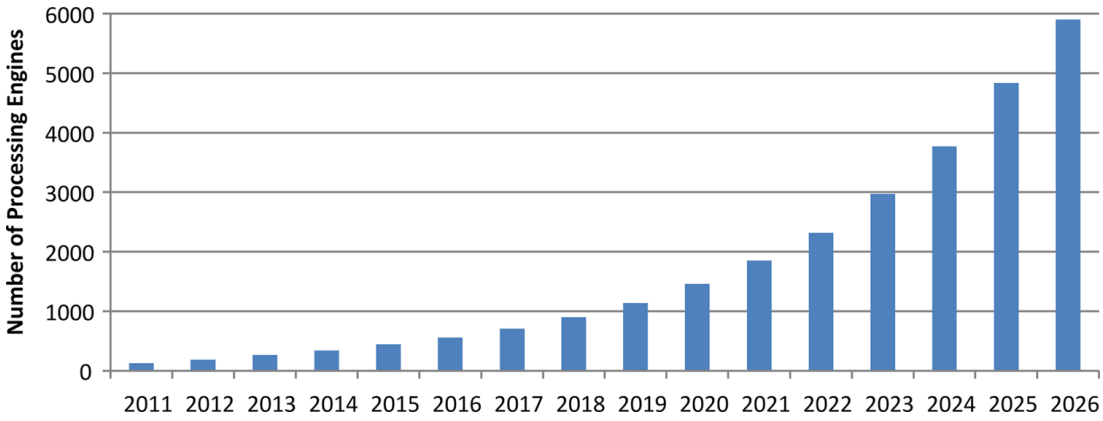
Tremendous steps forward in improving the density of silicon integration in recent years have introduced significant challenges for system engineers. An increasing number of new features have been integrated while development and implementation cycles have simultaneously decreased. This System on Chip (SoC) design complexity trend for portal devices is highlighted by Figure 1, as presented by the International Technology Roadmap for Semiconductors (ITRS Working Group, 2012, ITRS). Apart from consumer electronics, such highly integrated portable SoCs are also used in critical fields with high reliability and security demands. Because of this ever-increasing complexity, exhaustive test coverage of novel designs is difficult to achieve. As a consequence, support of system designers is needed during the whole design phase to test new hardware and software designs for possible weaknesses, as outlined by Ravi et al. (2004).

In addition to design flaws caused by complexity, there is the increasing fault probability provoked by deep sub-micron silicon integration technologies, as outlined by the latest ITRS report (ITRS Working Group, 2012, ITRS). This is a major issue especially for high safety applications (e.g., automotive, space, aviation). Therefore, a wide variety of fault injection techniques have been developed during the last few years to test the resistance of hardware/software designs against random faults, cf. for example Leveugle (2007).

The portable SoCs' trend of complexity increase is accompanied by an increase of power consumption, as depicted by Figure 2. This power consumption increase introduces major problems in several aspects. For example, mobile devices come with a limited power budget due to the limitations of batteries: the higher the power consumption, the lower the operational time. As another example, state-of-the-art integrated circuits use low supply voltage levels. This low-voltage approach causes high changing electrical currents, which requires sophisticated power supply networks to cope with the dynamic impedance of the chip. This is especially a problem for energy harvesting systems such as contactless reader / smart card systems.

In addition to complexity and power consumption challenges, secure embedded systems face the problem of the potential leak of critical information through side channels. A device's power consumption, for example, may disclose such crucial information, because of its data dependency. Thus, an adversary is able to deduce the internal secrets simply by observing the device's power consumption.

Figure 1. Design complexity trend of portable SoCs



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