

Synthetic Neuron Implementations

Snorre Aunet

University of Oslo, Norway & Centers for Neural Inspired Nano Architectures, Norway

S

INTRODUCTION

Many different synthetic neuron implementations exist, that include a variety of traits associated with biological neurons and our understanding of them. An important motivation behind the studies, modelling and implementations of different synthetic neurons, is that nature has provided the most efficient ways of doing important types of computations, that we are trying to mimick.

Whether it is Artificial Neural Networks (ANNs) or other mixed signal systems, technology has always evolved in the direction of lower energy per unit computation (Mead, 1990). Simple Neuron models as threshold elements, or perceptrons, are promising candidates for implementing future signal processing systems, including CMOS and SET (Schmid & Leblebici, 2003), (Beiu & Ibrahim, 2007).

In this article a small number of published sub-threshold, ultra low power, perceptrons / threshold elements are compared regarding power consumption, operational speed and defect tolerance. The “mirrored” gate operating in subthreshold and combined with redundancy, might be an interesting candidate for implementing artificial neural networks as well as other mixed-signal processing circuitry.

Previously unpublished results demonstrate the mirrored gate producing appropriate binary outputs at 180 mV supply voltage, even when a transistor was cut off the supply voltage, for a redundancy factor of 2, using shorted outputs, as in (Aunet & Hartmann, 2003).

BACKGROUND

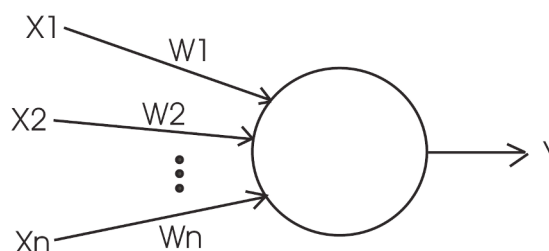
CMOS has been the dominant technology for implementing signal processing systems for decades, and will probably live alongside other nanotechnologies for a long time (ITRS, 2005). Due to needs for low power operation for about any future signal processing technology and that CMOS and similar technologies probably will be mainstream for the foreseeable future,

the scope of this paper is limited to simple CMOS, ultra low power circuit topologies. Subthreshold circuits (Swansson & Meindl, 1972), using a supply voltage below the inherent threshold voltage of the transistors, consume less power than other low power circuits (Soeleman, Roy & Paul, 2001). Therefore we look at subthreshold neuron (“perceptron”) implementations in this paper, and concentrate on different metrics including circuit complexity, operational speed, power consumption and defect tolerance.

Reducing the power supply voltage through using ever more modern CMOS technologies and subthreshold operation reduces the number of inputs one could use for the threshold elements, depicted in Figure 1 (Aunet, 2002). Also, since only 2 inputs is optimal to implement any arbitrary neural network (Beiu & Markaruk, 1998) we have restricted the treatment to basic building blocks having a maximum fan-in of 3.

The first simple mathematical model of the biological neurons, published by McCulloch and Pitts in 1943, calculates the sign of the weighed sum of inputs. Sometimes such circuits are called threshold logic gates or threshold elements, illustrated in Figure 1. Such perceptrons may be used to implement Neural Networks as well as digital signal processing. For a review on a wide range of VLSI implementations the reader might confer (Beiu, Avedillo & Quintana, 2003).

Figure 1. The binary output, Y , depends on if the weighted sum of inputs X_1, X_2, \dots, X_n exceeds a certain Threshold, T .



ULTRA LOW POWER NEURONS, SPEED AND RELIABILITY

The main focus is on different subthreshold ultra low power perceptrons and how they compare regarding power consumption, operational speed and reliability.

MOS Transistors in Subthreshold

For an NMOS transistor in subthreshold we have (Andreou, Boahen, Pouliquen, Pavasovic, Jenkins & Strohhahn, 1991):

$$I_{ds,n} = I_0 e^{(\kappa V_{gs}/V_t)} e^{((1-\kappa)V_{bs}/V_t)} (1 - e^{(-V_{ds}/V_t) + V_{ds}/V_0})$$

$I_{ds,n}$ expresses the current from drain to source. I_0 is the zero-bias current where the pre-exponential constants have been absorbed. This includes the channel width (“W”) and the length (“L”) of the MOSFET structure. V_{gs} is the gate-to-source potential, V_{ds} the drain-to-source potential and V_{bs} the substrate-to-source potential.

V_0 is the Early voltage, which is proportional to the channel length. κ gives the effectiveness for which the gate potential is controlling the channel current. It is often approximately 0.7-0.75 (Andreou, Boahen, Pouliquen, Pavasovic, Jenkins & Strohhahn, 1991). The thermal voltage is expressed as $V_t = kT/q$. $V_t = 25.8$ mV at room temperature.

A similar equation apply to PMOS transistors, but with opposite polarities. Exponential relationships

between voltages between several nodes and the current level mean that subthreshold circuits also have operational speed and power consumption that are extremely dependent on the supply voltage, V_{dd} . For example when operated at 10 kHz a subthreshold circuit used four orders of magnitude less than a regular strong inversion circuit implementing the same function (Soeleman, Roy & Paul, 2001).

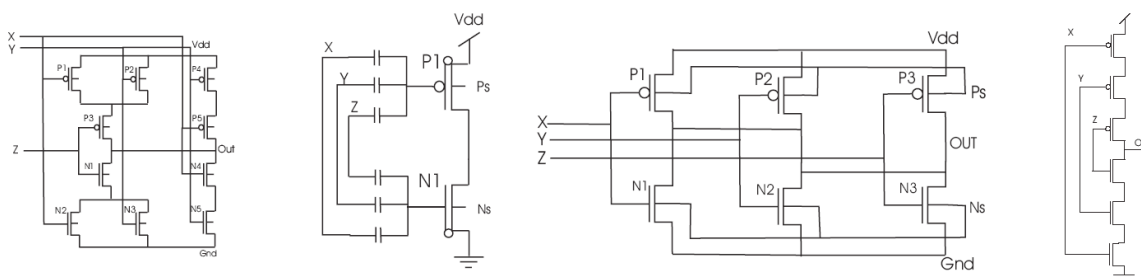
Low Fan-In Subthreshold Threshold Element (“Neuron”) Circuit Implementations

Recently published circuits are shown in Figure 2. The “mirrored gate” is a static CMOS solution (Beiu, Aunet, Nyathi, Rydberg III & Djupdal, 2005), based on (Hampel D., Prost K. J. & Scheinberg N. R., 1974). The floating-gate solution P3N3 (Aunet, 2002) might not go well along with future standard CMOS due to gate leakage, while the “ijcnn” (Aunet, Oelmann, Abdalla & Berg, 2004) and “stacked” (Aunet, Berg & Beiu, 2005) gates are CMOS.

Metrics Regarding Power Consumption and Maximum Operational Speed

Recently published results are shown in Figure 3 (Granhaug & Aunet, 2006). The “mirrored”, “ijcnn” and “stacked” gates were used for implementing 1-bit addition, Full Adders, in a 90 nm CMOS technology, and compared to a standard CMOS implementation (upper right corner in Figure 4).

Figure 2. Experimental setup for statistical simulation of 1-bit adder. From left to right they are called “mirrored”, “P3N3”, “IJCNN” and “Stacked” threshold elements.



5 more pages are available in the full version of this document, which may be purchased using the "Add to Cart" button on the publisher's webpage: www.igi-global.com/chapter/synthetic-neuron-implementations/10445

Related Content

Computing Optimization of a Parallel Structure-Based Monolithic Gripper for Manipulation Using Weight Method-Based Grey Relational Analysis

Ngoc Le Chau, Nhat Linh Ho, Tran The Vinh Chung, Shyh-Chour Huang and Thanh-Phong Dao (2021). *International Journal of Ambient Computing and Intelligence* (pp. 39-74).

www.irma-international.org/article/computing-optimization-of-a-parallel-structure-based-monolithic-gripper-for-manipulation-using-weight-method-based-grey-relational-analysis/279585

Patient Data Privacy and Security in the Healthcare Industry

Rohitha Sai Manne, Pramod Sai Gandla, Nikhil Shekhar Reddy and Pokala Pranay Kumar (2025). *AI-Driven Breakthroughs in Antimicrobial Resistance* (pp. 325-340).

www.irma-international.org/chapter/patient-data-privacy-and-security-in-the-healthcare-industry/374869

AI-Powered ChatGPT in Education: A Double-Edged Sword

Rahul Joshi, Suman Kumari and Krishna Pandey (2025). *Enhancing Learning Experiences With Digital Tools: AI, ChatGPT, and Virtual and Augmented Reality* (pp. 47-74).

www.irma-international.org/chapter/ai-powered-chatgpt-in-education/372163

Coordinative Optimization Control of Microgrid Based on Model Predictive Control

Changbin Hu, Lisong Bi, ZhengGuo Piao, ChunXue Wen and Lijun Hou (2018). *International Journal of Ambient Computing and Intelligence* (pp. 57-75).

www.irma-international.org/article/coordinative-optimization-control-of-microgrid-based-on-model-predictive-control/204349

Applying Semantic Web Technologies to Ontology Alignment

Hayden Wimmer, Victoria Yoon and Roy Rada (2012). *International Journal of Intelligent Information Technologies* (pp. 1-9).

www.irma-international.org/article/applying-semantic-web-technologies-ontology/63348