Statistical Simulations on Perceptron–Based Adders

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INTRODUCTION

In this article we compare a number of full-adder (1-bit addition) cells regarding minimum supply voltage and yield, when taking statistical simulations into account. According to the ITRS Roadmap two of the most important challenges for future nanoelectronics design are reducing *power consumption* and increasing *manufacturability* (ITRS, 2005).

We use subthreshold CMOS, which is regarded by many as the most promising ultra low power circuit technique. It is also shown that a minimum redundancy-factor as low as 2 is sufficient to make circuits maintain full functionality under the presence of defects. This is, to our knowledge, the lowest redundancy reported for comparable circuits, and builds on a method suggested a few years ago (Aunet & Hartmann, 2003).

A standard Full-Adder (FA) and an FA based on perceptrons exploiting the "mirrored gate", implemented in a standard 90 nm CMOS technology, are shown not to withstand statistical mismatch and process variations for supply voltages below 150 mV. Exploiting a redundancy scheme tolerating "open" faults, with gate-level redundancy and shorted outputs, shows that the same two FAs might produce adequate Sum and Carry outputs at the presence of a defect PMOS for supply voltages above 150 mV, for a redundancy factor of 2 (Aunet & Otnes Berge, 2007).

Two additional perceptrons do not tolerate the process variations, according to simulations. Simulations suggest that the standard FA has the lowest power consumption. Power consumption varies more than an order of magnitude for all subthreshold FAs, due to the statistical variations.

BACKGROUND

The first simple mathematical model of the biological neurons, published by McCulloch and Pitts in 1943, calculates the sign of the weigthed sum of inputs. Sometimes such circuits are called threshold logic gates or threshold elements. Perceptrons may be used to implement Neural Networks as well as digital signal processing.

Nanoscale CMOS technology is expected to be used alongside other technologies in the future. A typical chip will fail if even a single transistor or wire on the chip is defective. Reducing the power consumption and making defect tolerant circuits have been pointed out as important issues (Mead, 1990), (ITRS, 2005).

Reducing the power supply voltage is the most direct and dramatic means of reducing the power consumption (Liu & Svensson, 1993), and subthreshold circuits operating with a supply voltage, V_{dd}, less than the absolute value of the inherent threshold voltages, Vt, has been known for decades (Swensson, Meindl, 1972).

For older technologies, where manufacturability including threshold voltage variability, was not such an important issue (ITRS 2005),(Wong, Mittal, Cao & Starr, 2004) the minimum supply voltages have often been estimated without mismatch and process variations being taken into account (Liu & Svensson, 1993),(Schrom & Selberherr, 1996). To get more realistic estimates we have simulated and compared 4 different topologies for 1-bit addition under statistical variations in the process and matching properties.

MAIN FOCUS OF THE CHAPTER

MOS Transistors in Subthreshold

For an NMOS transistor in subthreshold we have (Andreou, Boahen, Pouliquen, Pavasovic, Jenkins & Strohbehn, 1991):

$$I_{ds,n} = I_0 e^{\frac{\kappa V_{gs}}{V_t}} e^{(1-\kappa)\frac{V_{bs}}{V_t}} \left(1 - e^{-\frac{V_{ds}}{V_t}} + \frac{V_{ds}}{V_0} \right)$$

$I_{ds,n}$ expresses the current from drain to source. I_0 is the zero-bias current where the pre-exponential constants have been absorbed. This includes the channel width ("W") and the length ("L") of the MOSFET structure. V_{gs} is the gate-to-source potential, V_{ds} the drain-to-source potential and Vbs the substrate-to-source potential.

V_0 is the Early voltage, which is proportional to the channel length. κ gives the effectiveness for which the gate potential is controlling the channel current. It is often approximately 0.7-0.75 (Andreou, Boahen, Pouliquen, Pavasovic, Jenkins & Strohbehn, 1991). The thermal voltage is expressed as $V_t = kT/q$. $V_t = 25.8$ mV at room temperature.

Though equation (1) takes fewer physical effects and nonmonotonous behaviour in certain cases into account, than for example that reported in (Calhoun, Wang & Chandrakasan, 2004), it does provide sufficient insight to make a brief analysis of many subthreshold circuits. A similar equation apply to PMOS transistors, but with opposite polarities.

Experimental Setup for Statistical Simulations of Functionality and Power Consumption for 1-Bit Adders

For statistical (Monte-Carlo) simulations we used a 90 nm standard CMOS process available through CMP (CMP, 2007). Four different Full Adder ("FA") circuits having their inputs driven by inverters, and themselves driving simple inverters were simulated. This is illustrated in figure 1. In the case of no redundancy and faults the lower FA in figure (1) was not included.

For each circuit, at 8 different supply voltages, 100 Monte-Carlo "runs" were done, each having the eight possible combinations of the three inputs, for a total simulated period (transient simulation) of 400 μs, as illustrated in figure 3 for a case after 5 "runs". This was far from the maximum operational speed of any of the FAs, meaning that the resulting Sum and Carry signals had more than enough time to settle. Each of the 100 runs represented different mismatch and process parameters, and for each run we checked if the circuit was able to produce correct "0" or "1" outputs for all eight input combinations. The yield, shown in figure 4 represents the percentage of the Full Adders (FAs) working for a given supply voltage, out of 100 Monte Carlo "runs".

Redundancy using short circuited driven nodes (Aunet & Hartmann, 2003) was exploited, duplicating each gate for the three FAs based on threshold gates (figure 2). For the other FA only the driven nodes prior to the inverters preceeding the S and C nodes were shorted. A total of 4 PMOS transistors were removed from the 4 FAs (one for each FA), so that each FA missed one PMOS in one of it's threshold gates. This means that each FA in figure 1 had exactly (2N -1) the number of transistors, N, when compared to the previous case with no redundancy.

The average power consumption for the eight input combinations was also calculated. Each of the four circuits perceptrons, with no redundancy, was tested for 8 different supply voltages.

The missing transistor was in the lowermost "min3" gate (figure 2). For the mirrored gate the missing PMOS was the one having the Z input. For the stacked gate as well as the ijcnn gate the missing PMOS was the one between the two other PMOS transistors, referred to figure 2.

For the FA in the upper left corner of figure 2 a PMOS with it's gate connected to the C_{in} input was the one that was removed. Regarding the rest of the setup it was identical to the one in the previous subsection, describing the case without redundancy.

The FAs put to test were a standard CMOS Full Adder containing 28 transistors (upper, left, in figure 2), while the three others were based on the topology in the upper, right, corner of figure 2. They were based on, from left to right in figure 2, the "mirrored gate" (Hampel, Prost & Scheinberg, 1974), the "stacked" gate (Aunet, Berg & Beiu, 2005) and the "ijcnn" gate (Aunet, Oelmann, Abdalla & Berg, 2004), which are all threshold gates.

Regarding transistor dimensions all gate lengths were 100 nm, and all NMOS widths were 220 nm. The standard FA and the "stacked" FA had widths of

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