A Novel Prototyping and Evaluation Framework for NoC-Based MPSoC

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ABSTRACT

This paper presents a framework for high-level exploration, Register Transfer-Level (RTL) design and rapid prototyping of Network-on-Chip (NoC) architectures. From the high-level exploration, a selected NoC topology is derived, which is then implemented in RTL using an automated design flow. Furthermore, for verification purposes, appropriate self-checking testbenches for the verification of the RTL and architecture files for the semi-automatic implementation of the system in Xilinx EDK are also generated, significantly reducing design and verification time, and therefore Non-Recurring Engineering (NRE) cost. Simulation and FPGA implementation results are given for four case studies multimedia applications, proving the validity of the proposed approach.

Keywords: Field-Programmable Gate Array (FPGA), High-Level Exploration, Network-on-Chip (NoC), NoC Prototyping, Three-Dimensional (3D) Chips

INTRODUCTION

Future integrated systems will contain billion of transistors (Semiconductor Industry Association, 2011), composing tens to hundreds of IP cores. These systems will host emerging multimedia and network applications, should be able to deliver rich multimedia content and networking services. An efficient cooperation among these IP cores (e.g., efficient data transfers) can be achieved through utilization of the available resources.

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An architecture being able to accommodate such a high number of cores, satisfying the needs for efficient communication and bandwidth, is the Network-on-Chip (NoC) (Benini & de Micheli, 2002; Jantch & Tenhunen, 2003). For these reasons Networks-on-Chip become a popular choice for designing the on-chip interconnect for Systems-on-Chip (MPSoCs), and are supported from the industry (implementations such as the AEthereal NoC (Kumar, Hansson, Huisken, & Corporaal, 2007) from Philips, the STNoC (STMicroelectronics, 2005) from STMicroelectronics and an 80-core NoC from Intel (Vangal, S. Howard, J., Ruhl, G.; Dighe, S., Wilson, H., Tschanz, J., Finan, D., Iyer, P., Singh, A., Jacob, T., Jain, S., Venkataraman, S., Hoskote, Y. & Borkar, N., 2007)). The design of such complex systems includes several challenges to be addressed. Among others one challenge is to design an on-chip interconnection network that should be able to efficiently connect the IP cores. Another challenge is to derive such an application mapping that will make efficient usage of the available hardware resources (Murali & De Micheli, 2004; Hu & Marculescu 2005). Furthermore, verification of such systems is a very complicated task.

The on-chip interconnection is a widely studied research field and good overviews are (Dally & Towles, 2003; Duato, Yalamanchili, & Lionel, 2002), illustrating the various interconnection schemes available for present ICs and emerging Multiprocessor Systems-on-Chip (MPSoC) architectures. In Lee, H. G., Chang, N., Ogras, U. Y., & Marculescu, R. (2007) a quantitative evaluation of point-to-point, bus and NoC interconnection approaches is presented. In this work four case studies are explored, one is a mesh topology MPEG-2 implementation while the other is an irregular topology multimedia implementation. The case studies demonstrate that the proposed flow works well for both regular and irregular NoC topologies.

The paper is organized in seven sections: The next section summarizes previous related work, the third section describes the high-level exploration methodology, while the fourth section describes the RTL NoC components and the fifth the tool for the automatic generation of RTL and rapid prototyping. The sixth section provides experimental results and discussion. The paper concludes with the seventh and final section.

**PREVIOUS WORK**

A number of NoC architectures have been implemented and evaluated in both FPGA and ASIC platforms, among them (Ehliar & Liu, 2007; Genko, Atienza, & De Micheli, 2005). Furthermore, frameworks and tools for high-level exploration for NoC architectures exist (Kumar, Hansson, Huisken, & Corporaal, 2007).

In Leary and Chatha (2010) a holistic algorithm for NoC synthesis able to address all these requirements together in an integrated manner was presented. However, the synthesis methodology provided does not provide Register Transfer-Level descriptions that can readily be used for system implementation.


FPGA rapid prototyping has been explored in Ogras, Y., Marculescu, R., Lee, H. G., Choudhary, P., Marculescu, D., Kaufman, M., & Nelson, P. (2007), where using FPGA long links was explored, however, the authors mention having to modify a router manually to insert long links, requiring less than a day. In the proposed framework, this modification would have been trivial, due to the automatic RTL generation tool. Similarly, a 3×3 mesh NoC for an image processing benchmark was implemented in Le, T., and Khalid, M. (2009). In Krasteva, Y.E., Criado, F., de la Torre E., and Riesgo, T. (2008) a more flexible prototyping framework was presented, which includes RTL NoC models and also supports dynamic reconfiguration. However, our framework also includes design space exploration starting from...
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