A Performance Prediction Method with an Equation-Based Behavioral Model for a Single-Bit Single-Loop Sigma-Delta Modulator

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ABSTRACT

An equation-based behavioral model has been developed to predict the real performance of a single-loop single-bit Sigma Delta Modulator (SDM). By using this prediction flow, not only can the circuit specifications be acquired, including the gain, bandwidth, slew rate of the OPAMPs, and the capacitor value in the switched-capacitor circuits, but the real performance of the SDM can also be predicted. The switched-capacitor circuits according to the required circuit specifications are employed to design a fourth-order feed-forward (FF) SDM with an over-sampling ratio (OSR) of 64 and a bandwidth of 10kHz using a TSMC 0.35μm CMOS process. The measurement results reveal that the SDM with an input frequency of 2.5kHz and a supply voltage of 3.3V can achieve a dynamic range of 90dB and a spurious-free dynamic range (SFDR) of 85dB under the signal bandwidth of 10kHz and a sampling frequency of 1.28MHz, respectively. The precision of the equation-based behavioral model has been validated by experimental measurements, and its inaccuracy is less than 4%.

Keywords: Behavioral Model, Equation-Based, Feed-Forward (FF), Over-Sampling Ratio (OSR), Sigma Delta Modulator (SDM), Spurious-Free Dynamic Range (SFDR)

1. INTRODUCTION

In recent years, analog to digital converters (ADCs), including pipeline, successive approximation, flash, and sigma-delta structures, are fairly popular for system-on-a-chip (SOC) applications. Among them, sigma-delta analog-to-digital converters (SDADCs) have become more widely used in hearing aid, digital audio, and broadband network systems because the resolution requirement can be easily achieved by a sigma-delta modulator (SDM) with over-
sampling and noise-shaping techniques. SDM can also relax the design of an anti-alias analog filter and further reduce the power consumption of the analog front-end circuits (Rabii & Wooley, 1997). SDADC is traditionally composed of an analog SDM and a digital decimation filter implemented by a finite impulse response (FIR) filter or by an infinite impulse response (IIR) filter (Lee and Cheng, 2006). Difference to an analog modulator, the digital filter is more easily implemented because of the reliability of digital circuits. However, in an analog modulator, the performance will be dominated by non-ideal effects in the circuit implementation.

There are several good models used to analyze SDM. For instance, Francken found the best architecture and requirements for the building blocks to fit a specification, and therefore, the behavioral model including non-ideal effects should be built and applied to the system simulation to obtain the required circuit specifications (Francken & Gielen, 2003). In this paper, the non-ideal behavioral models including clock jitter, thermal noise, operational amplifier (OPAMP) finite gain and nonlinearity, OPAMP bandwidth and slew rate, nonzero switched-on resistance, and noise budget have been presented, and the required circuit specifications can also be produced. These non-ideal effects have been incorporated into one SIMULINK model, and it can be used to predict the real performance of SDM. Based on these analyses, a switched-capacitor (SC) fourth-order SDM has been implemented in the TSMC 0.35μm CMOS process to demonstrate the proposed equation-based behavioral model.

The rest of this paper is organized as follows. Section 2 presents the performance prediction issues, introduces the behavioral models with an equation-based method, and produces the systematic design flow. The circuit implementation and measured results will be described in Section 3 and Section 4, respectively, to demonstrate the behavioral model. Finally, Section 5 briefly concludes this paper.

2. PERFORMANCE PREDICTION ISSUES

Figure 1 shows the proposed prediction flow of SDM performance. According to this flow, the real performance can easily be predicted, and the required specification of the building blocks in SDM can be obtained. First the specifications of SDM, including bandwidth, peak signal-to-noise ratio (PSNR), and maximum input range, should be defined, and then the designer can alter the oversampling ratio (OSR) and fit the required coefficients of the selected architecture according to the stability requirement. To tolerate the performance degradation of SDM as considering all the non-ideal circuit effects (Malcovati et al., 2003), the next step is to create the circuit behavioural model with SIMULINK and individually apply it to the SDM architecture in order to obtain the required circuit specifications. When acquiring the detailed specifications, the non-ideal effects can be integrated into the SDM with consideration of all the non-ideal effects at the same time. Therefore, the real SNR and dynamic range (DR) can be predicted by the proposed integrated behavioral model. According to this procedure, the designers can rapidly predict the real performance before the circuit implementation. If the final simulation results do not match the required system specification, the designers can try to revise the specification in order to tolerate the performance degradation caused by the circuit implementation.

The application applied in the hearing aid (Gata et al., 1997) is adopted as the design example, where the system has an effective number of bits (ENOB) of about 14-16 bits, a bandwidth (BW) of 10kHz, and an OSR of 64, and then the required SDM coefficients adopting feed-forward (FF) and multiple-feedback (MF) structures can be synthesized (Kuo et al., 1999; Norsworthy et al., 1997). In this paper, the inverse-Chebyshev high-pass function is adopted to synthesize the noise transfer function (NTF) and employed in a fourth-order FF SDM structure as shown in Figure 2, where the NTF
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