Chapter 13
Task Migration in Embedded Systems: Design and Performance

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ABSTRACT

Task migration has a great consideration is MPSoC design and implementation of embedded systems in order to improve performance related to optimizing execution time or reducing energy consumption. Multi-Processor Systems-on-Chip (MPSoC) are now the leading hardware platform featured in embedded systems. This chapter deals with the impact of task migration as an alternative to meet performance constraints in the design flow. The authors explain the different levels of the design process and propose a methodology to master the migration process at transaction level. This methodology uses some open source tools like SDF3 modified to provide performance estimation at transaction level. These results help the designer to choose the best hardware model in replacement of the previous software implementation of the task object of migration. Using the SDF3 tool, the authors model a multimedia application using SDF graphs. Secondly, they target an MPSoC platform. The authors take a performance constraint to achieve 25 frames per second.

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INTRODUCTION

Currently, multimedia applications have important computation needs, and induce high transfers of data. They will do much more than just playback pre-recorded audio and video; they will employ sophisticated image processing techniques and integrate complex computer graphics, all delivered with high interactivity and real-time response. Furthermore, multimedia applications are composed of several independent tasks that can run in an autonomous way as soon as they have the appropriate input data at their input points.

To fulfill the need for computation, while ensuring correct performances, designers often have resort to software-to-hardware tasks migration. But when implementing applications on MPSoC systems, migrating software tasks to hardware tasks is a costly process. One of the ways to avoid such expenses is performance estimation at different design levels.

The general problematic needed to be answered is how to help a designer to estimate the performances of an application which have to be executed on an MPSoC platform, at design level. This chapter specifically targets performance estimation of software-to-hardware migration on MPSoC systems with SDF graphs. The first section of this chapter presents the state of the art on performance estimation of MPSoC systems. The second section describes an approach for performance estimation of MPSoC systems with SDF graphs. The experimentations are presented in details in the third section, through the case study of a MPJEG decoder. The chapter ends with a conclusion and a glimpse of the work perspectives.

1. STATE ART OF PERFORMANCE ESTIMATION IN MPSOC DESIGN

Several research projects already tackle the subject of performance estimation of migration on MPSoC systems. Indeed, recently, research is more and more concerned with the use of the Synchronous Data Flow (SDF) graph in the MPSoC design. Jerraya (2008) points out that NoC-MPSoC design is the subject of more than 60 research projects over the world.

For their part, Kumar and al. (Kumar, Mesman, Theelen, Corporaal, & Ha, 2008) have proposed a solution to analyze applications that are modeled by SDF graphs and executed on MPSoC platform through the use of Resource Manager (RM). RM is a task which controls and directs the use of resources. It is responsible for resources access (critical or not), and optimization of their usage. The designer reserves for the RM a whole execution node (CPU, memory, bus ...) which increases the cost of the total MPSoC system.

Lahiri and all (Lahiri, Raghunathan, & Dey, 2000) presented methodologies and algorithms to design communication architectures in order to achieve the desired performance on MPSoC systems. They developed a tool named Communication Analysis Graph (CAG), which relies on SDF graphs for MPSoC performance analysis and constraint satisfaction.

Wiggers and all (Wiggers, Kavaldjiev, Smit, & Jansen, 2005) proposed a solution that consists in mapping purely software tasks and their communication channels on the target processors. They exploited the SDF graphs to compare the throughput obtained with the target throughput of the application. Finally, S. Stuijk (2007) proposed a design flow for mapping multimedia applications on NoC-MPSoC platforms.

2. AN APPROACH FOR PERFORMANCE ESTIMATION OF MPSOC SYSTEMS WITH SDF GRAPHS

We propose in this chapter a methodology for performance estimation of MPSoC systems with SDF graphs, which is called the methodology for software-to-hardware migration performance