Chapter 2
SOI Technology in Designing Low-Power VLSI Circuits

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ABSTRACT

At present, the transistor size is reduced to a few tens of nanometers, as larger transistors demand a large die area and power. Power is an important design parameter in multi-gigahertz communication and ASIC/SOC designs. To deliver higher performance with lower power, various technologies are adopted in semiconductor industry. SOI is one such technology that helps in achieving higher performance. It offers a platform to integrate digital and RF circuit onto a single chip. Adopting SOI technology, faster chips with lesser power can be designed. This extends the battery life of handheld devices. The SOI structure is comparable to MOSFET except for an added buried oxide (Box) layer beneath the device region. The Box layer isolates the top and the base silicon layers and reduces the junction capacitances. This reduction accelerates the speed, lowers the power consumption, allows higher transistor stacking, and improves the device performance. These capabilities have led SOI usage in RF circuits. This chapter discusses the SOI technology in building energy- and power-efficient designs.

INTRODUCTION

The increase in the demand for compact portable electronic devices has given room for inventing number of techniques to reduce the power consumption while

DOI: 10.4018/978-1-6684-4974-5.ch002

delivering the same performance. This has paved way in investing lot of time and effort in developing low power techniques for computation intensive applications.

In recent days, SOI is grabbing a lot of interest in high-performance circuits design. It offers higher speed, low power, reliability and hardness well beyond the traditional technologies. The superior performance of SOI can be attributed to overall reduction in the capacitance and to lower device leakage. This paves way for using SOI in sophisticated IC designs working under Low Power-Low voltage conditions.

Devices built over Silicon on Insulator (SOI) wafer offers many potential benefits in microelectronics compared to the devices built on bulk silicon which has more volume of semiconductor material underneath the device and demands more charge to turn it on and off. The relative advantages of SOI wafers will be higher when operating at lower voltages (Kononchuk & Nguyen, 2014). SOI technology also minimizes the parasitic bipolar latch up effects. Reduction in latch up has reduced the size of the transistor and has increased the packaging density. For mixed signal and radio frequency applications, SOI technology offers lower noise and higher quality passives. Further cross talk can be reduced using ground plane silicon on insulator that is formed by incorporating silicide layers. These advantages of SOI technology is obtained owing to two key features:

a. Reduction of junction parasitic capacitance.
b. Total dielectric separation of the transistor elements.

SOI CONSTRUCTION, PRINCIPLES AND FEATURES

As SOI paves way to reduce the power requirements and accelerates the operational speed, it is now being used in hand held battery operated devices. SOI CMOS has 25% higher switching speed and approximately three times lesser power consumption than similar circuits built on bulk silicon. These improvements obtained using SOI CMOS is comparable to benefits obtained after one or two generations of transistors scaling built using bulk silicon.

SOI structure has a base layer which is a standard silicon wafer. It only provides the mechanical support to the structure. An insulation layer called buried oxide (BOX) layer and a very thin top layer of silicon film is then deposited on the base layer. All the functional structures are formed only in the top layer of thin silicon that is placed above the insulator. Each MOS device that is formed in the top layer is separated by surrounding BOX as shown in Figure 1. Hence neither a separate well nor field oxide deposition is required to electrically isolate the devices as in conventional CMOS structures. The silicon substrate is isolated from the top thin