# Chapter 1
# Low-Power Methodologies and Strategies in VLSI Circuits

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## ABSTRACT

*Due to the fact that low-power gadgets are currently dominating the electronics sectors, researchers are studying their design. Power management is a crucial parameter for designing VLSI circuits since it is essential for estimating the performance of devices, especially those utilized in biomedical and IoT applications. To achieve greater performance, designing a low-power system on a IC is becoming increasingly challenging due to the reduction in size of chip, increases in chip density, and rise in device complexity. Furthermore, for the less than 90 nm node, due to its increasingly complicated design, the total power factor on a chip is turning into a significant difficulty. Leakage current also has a significant effect on how low-power VLSI devices manage their power. Leakage and dynamic power reduction are increasingly being prioritized in VLSI circuit design in order to improve the battery life of electronic portable devices. The many methodologies, tactics, and power management schemes that can be employed for the design of low-power circuit systems are discussed in this chapter.*

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## INTRODUCTION

Since the transistor era, which laid the groundwork for low-power consuming gadgets, the microelectronics industry has experienced a significant boom. The electronic components (IC) reduced size while also enhancing the circuits' performance. This causes the area of the power in the components to increase. There is a great demand for low power consuming gadgets is driven by a striking increase in battery oriented complicated life rescuing devices. Nowadays more concentration is to develop low power devices and design methodologies. On the other hand, with high power consumption devices, the silicon failure rate doubles for every 10-degree increase in temperature. As deep submicron nodes and nanoscale technologies advanced, the unprecedented development of power reduction gained significance.

Very-Large-Scale Integration is a technique that builds an integrated circuit (IC) by fusing thousands of transistors with other devices onto a single chip. Today, designing low power consumption is the top priorities for intricate very large-scale integration (VLSI) circuits. Table 1.1 lists various VLSI technology and its representation. Evolution of IC Technology précised in Table 1.2.

Rapid and creative advancements in low-power design have occurred recently rising the popularity of mobile devices. Hence, there is a necessity to reduce power consumption in very-high density chips. The motivations for these advances include portable applications such laptops, portable devices, and personal digital assistants that require low power consumption and high throughput. In these situations, it is necessary to achieve both the challenging objectives of high chip density and throughput in addition to the low power consumption requirements. As a result, the field of CMOS design for low-power digital integrated circuits has become quite active and is expanding very quickly.

Low-power consumption in digital systems, achieved using a variety of approaches, ranging from device to algorithm level. Reduced power consumption is mostly a result of device parameters (such as threshold voltage), device geometries, and connection qualities. To reduce power dissipation at the transistor level, circuit-level techniques can be utilized. Circuit-level includes the selection of circuit design styles appropriately, lowering the voltage change, and clocking methods. Smart management of power technique of different blocks, the use of pipelining, parallelism, and the bus structure are examples of architecture-level controls. Finally, system power consumption can be reduced by carefully choosing the data processing algorithms and limiting the amount of switching events for a given activity.

Performance of a processor measured as million instructions per second (MIPS), has previously been equated with processing power or circuit speed. When designing ICs, power consumption was only a minor consideration. However, power has emerged as the most crucial issue in nanoscale technology due to: