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Wrapped Channel FET (WCFET): Future of Low Power Application

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ABSTRACT

In this article, the authors examined the electrical characteristic of proposed new device structure, wrapped channel field effect transistor (WCFET). Results of WCFET have been analyzed using Atlas 3-D simulator. WCFET shows better transfer characteristics with ON-current ION of ~10-6A and leakage current IOFF of ~10-16 A. Optimization of device characteristics is done with doping concentration (ND), gate work function (ΦG), and spacer dielectric. Impact of gate length and semiconductor film thickness variation on drain current, subthreshold slope (SS), and DIBL are also investigated. Further, effects of various gate dielectric materials such as SiO2, Si3N3, HfO2, and TiO2 are examined w.r.t. switching characteristics of WCFET. To validate of device compatibility with power supply scaling, the authors inspected full range variation of VDS ≈ (0.05V-to-0.7V) on transfer characteristics.

KEYWORDS

FINFET, Junctionless FETs, SOI, WCFET, Wrapped Channel

1. INTRODUCTION

To meet the demand of semiconductor market, the density of transistors in a chip is increasing rapidly. The formation of ultra sharp and shallow source/drain, PN junction in multigate devices is challenging task for semiconductor technologists. So researchers started searching for alternative solution of these bottlenecks. Gate -all-around junction less FET(GAA-JLFET) is one of the most promising candidates for future CMOS technology due to their improved electrostatic control compared to double gate as well as bulk devices Morita (2013), Suzuki (1993), Frank (1998), Hu (1993), Li (2009), Ray (2008). However, it is limited by the scalability as fabrication procedure requires very high level of calibration and precision. Further, randomness added for less than 20nm process makes it unviable. Junctionless field-effect transistor is under evaluation as potential replacements for traditional planner transistors in upcoming sub-20 nm technology nodes. It is potential solution to random dopant fluctuation as it contains uniformly doped channel. Additionally, it has suppressed short channel effects and high

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switching speed Suzuki (1993). However, low improvement in sub threshold slope makes junctionless transistors power hungry devices and hinders junctionless FET (JLFET) from potential applications. There have been multiple attempts to optimize the power and performance trade-off using various approaches however, there's still scope of improvement [8-16]. This bottleneck can be solved using WCFET which highly suppresses leakage current. In this work, we have proposed a novel device structure, Wrapped Channel Field Effect Transistor (WCFET). The proposed device has several advantages such as better gate control, low leakage current (I_{OFF}) and easy fabrication process than junction-based devices such as double gate conventional MOSFETs, FINFET etc. WCFETs can be seen as seen as amalgamation of FINFETs and SOI structures, bringing advantages of both the models.

2. CONCEPT ADOPTION AND DEVICE SIMULATION DETAIL

Device structures of SOI FINFET and Wrapped Channel FET (WCFET) are shown in Fig 1. Wrapped channel structure is inverted form of FINFET. Instead of having single sheet of channel, channel is wrapped in three sides of gate maximizing current in per unit area at same level of gate control on drain current. This makes WCFET almost 3 times more effective than FINFET. The control over current is achieved using thin channel similar to SOI structures. As both the architectures work in junctionless mode hence in off state channel gets highly depleted while in on state, channel is partially depleted. The semiconductor film thickness is small enough to cause full depletion in OFF-state. This depletion is caused by the work function difference between gate electrode and highly doped channel. In OFF-state, depletion of highly doped channel causes electric field perpendicular to the direction of current flow. The field becomes zero above threshold as the conducting channel is neutral. Fig. (2 and 3) show axonometric view and cross-sectional view of electron concentration profile of FINFET and WCFET in OFF-state ($V_{DS} = 0.7$ V, $V_{GS} = 0.0$ V) and ON-state ($V_{DS} = 0.7$ V, $V_{GS} = 0.7$ V). Contrary to inversion mode devices these structures observe bulk current flow when device is switched ON. Table 1 depicts pre-set parameters. WCFET is based on very basic idea i.e. the leakage current becomes significant beneath gate electrode after 5nm depth or in other words, if channel thickness is less than 5nm then current would be highly controlled with insignificant leakage. This is established through our numerical simulations as well. We have simulated SOI FINFET with FIN of 5nm thickness, Ultra Thin Body (UTB) SOI with thickness of 5nm and SOI FINFET with FIN of 10nm thickness. All of them contain junctionless channel. FINFETs have FIN height of 30 nm and UTB has width of 30 nm. SiO_2 is used as dielectric with EOT of 2 nm and gate length 22 nm in all three structures. All the model parameters and structural parameters are kept same. The basic motive was to compare these structures for different film thicknesses. This is illustrated in Fig. 4 which compares ON-state current (I_{ON}), OFF- state current (I_{OFF}), ON-OFF current ratio (I_{ON}/I_{OFF}), Drain Induced Barrier Lowering (DIBL) and Sub-threshold Slope (SS). Clearly, I_{ON} is highly reduced in FIN with 5 nm thickness due to mobility degradation. This effect is lower in UTB of 5nm thickness as it contains single gate and hence it has better drive current. However, FIN with 10nm thickness has highest drain current because of more cross-sectional area and lesser mobility degradation. I_{OFF} is highly suppressed in 5nm FIN because of better gate control and mobility degradation. Therefore, I_{ON}/I_{OFF} is the highest observed in 5nm FIN. Moreover, it has minimum short channel effects due to better gate control. We observed that 5nm FIN provides better performance; however, 5nm UTB has comparative transfer characteristics with advantage of single gate per channel. Therefore, we coined WCFET device architecture which contains 5nm thick film around single gate. This structure has dual advantage of low budget fabrication process and area efficient structure than FINFET.

3. SIMULATIONS

Simulations are done in Device 3D, a SILVACO Device simulator. Drift-diffusion current transport model and Lombardi's model (CVT) are used for simulations Colinge (2010), Rahi (2015), Asthana

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