Chapter 3
Macro and Micro Architectures for Network on Chip: A Review

P. Suresh
https://orcid.org/0000-0002-0488-972X
Vel Tech Rangarajan Dr. Sagunthala R&D Institute of Science and Technology, India

ABSTRACT

Network on chip (NoC) paradigm replaces traditional, dedicated, and proprietary bus architectures of system on chip (SoC), and it is widely accepted by the system-level designers. In this chapter, an overview of the NoC design is presented in two different dimensions called macro-architectures and micro-architectures based on the design perspectives. Macro-architectures adopt the concept of computer network along with new innovations in topologies, protocols, and routing algorithms and so on whereas micro-architectures involve in the development of schedulers, arbiters, routers, and network adapter with existing or new concepts. From the comparison result, most of the NoC prototypes are developed with 2-D mesh architecture with packed switched concept. Apart from mesh architectures, some of the complex and hybrid concepts are also developed and discussed in this chapter.

INTRODUCTION

As the number of Processing Elements (PEs) in Systems-on-Chip (SoCs) increases, traditional on-chip communication architectures may prevent these systems to meet the required performance of many applications. For a SoC with multiple processors

DOI: 10.4018/978-1-7998-4610-9.ch003

Copyright © 2021, IGI Global. Copying or distributing in print or electronic forms without written permission of IGI Global is prohibited.

(Multiprocessor SoC - MPSoC), different on-chip communication architectures have been proposed to meet such requirements like high performance, flexibility, scalability, reliability, efficiency and so on. Rather than using a traditional on-chip communication architectures such as bus communication architectures, point-to-point communication architecture and crossbar architectures, other communication architectures have also been proposed to meet the on-chip communication requirements (Pasricha & Dutt, 2008). Figure 1 shows the different on-chip communication architectures for SoC or MPSoC. Figure 1 (a) shows the traditional bus based communication architecture for MPSoC. The main challenge using bus communication architecture is the bottleneck due to the bandwidth limitation (Pasricha & Dutt, 2008), (Dally & Towles, 2004). Figure 1 (b) depicts the fully crossbar communication architecture for MPSoC but it leads to higher electromagnetic interference and parasitic capacitance problems due to the metal interconnections. The dedicated point-to-point communication architecture used for MPSoCs is shown in Figure 1 (c), but the limitation is flexibility.

Figure 1 (d) shows the segmented bus based communication architecture for MPSoC, in which a bus communication system is interconnected with the other bus communication system using bridge. This type of bus communication system helps to overcome the bandwidth limitation of traditional bus communication architecture, but it leads to complex design and more timing consumption. However, since distributed bus arbitration corresponds to the cumulative actions of multiple arbitration units, computing optimal overall settings will be very complex and time consuming (Dally & Towles, 2004). The NoC is the promising solution for such problems and requirements with irregular and regular structures as shown in Figure 1 (e) and Figure 1 (f). The NoC consists of several routers used to route a packet sent by one PE to another. Therefore, the main attitude of the NoC is the development of communication architecture that enables to route the packets instead of the wires. The use of NoCs can be classified into two main categories, i.e. in embedded SoC applications domain commonly called MPSoC and in general-purpose microcomputer systems domain commonly called Chip-Level Multiprocessor (CMP) systems (Benini & Micheli, 2002).

29 more pages are available in the full version of this document, which may be purchased using the "Add to Cart" button on the publisher's webpage: www.igi-global.com/chapter/macro-and-micro-architectures-for-network-on-chip/271575

Related Content

Analysis of Bandwidth Efficiency in IEEE 802.11 and 802.16 Interworking Networks

Mateen Yaqooband Mustafa Shakir (2018). *International Journal of Wireless Networks and Broadband Technologies (pp. 25-38).*
www.irma-international.org/article/analysis-of-bandwidth-efficiency-in-ieee-80211-and-80216-interworking-networks/209433

M2M in 5G Communication Networks: Characteristics, Applications, Taxonomy, Technologies, and Future Challenges

Mohammed A. Salem, Sherine M. Abd El-Kader, Mohamed I. Youssefand Ibrahim F. Tarrad (2021). *Research Anthology on Developing and Optimizing 5G Networks and the Impact on Society (pp. 799-810).*
www.irma-international.org/chapter/m2m-in-5g-communication-networks/270217

SORT: A System for Adaptive Transmission of Video Over Delay Tolerant Networks

Abhishek Thakur (2020). *International Journal of Wireless Networks and Broadband Technologies (pp. 115-142).*
www.irma-international.org/article/sort/250910

Cloud-Based IoT Architecture for Green Buildings

Rejo Rajan Mathewand Vikram Kulkarni (2020). *Industrial Internet of Things and Cyber-Physical Systems: Transforming the Conventional to Digital (pp. 61-75).*
www.irma-international.org/chapter/cloud-based-iot-architecture-for-green-buildings/257840

Mobile Ad Hoc Networks Security Enhancement With Trust Management

Vaishali Vilas Sarbhukanand Lata Ragha (2021). *Managing Resources for Futuristic Wireless Networks (pp. 1-27).*
www.irma-international.org/chapter/mobile-ad-hoc-networks-security-enhancement-with-trust-management/262545