Chapter 2
CNTFET-Based Memory Design

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ABSTRACT

As the feature size of device has been scaling down for many decades, conventional CMOS technology-based static random access memory (SRAM) has reached its limit due to significant leakage power. Therefore, carbon nanotube field effect transistor (CNTFET) can be considered most suitable alternative for SRAM. In this chapter, the performance and stability of CNTFET-based SRAM cells have been analyzed. Numerous figures of merit (FOM) (e.g., read/write noise margin, power dissipation, and read/write delay) have been considered to analyze the performance of CNTFET-based. The static power consumption in CNTFET-based SRAM cell was compared with conventional complementary metal oxide semiconductor (CMOS)-based SRAM cell. Conventional CNTFET and tunnel CNTFET-based SRAMs have also been considered for comparison. From the simulation results, it is observed that tunnel CNTFET SRAM cells have shown improved FOM over conventional CNTFET 6T SRAM cells without losing stability.

DOI: 10.4018/978-1-7998-1393-4.ch002

1. INTRODUCTION

Over a few decades, as the integrated circuit (IC) technology has been growing rapidly, the feature size of transistors has dropped from micrometer to nanometer regime for having high packaging density on a single chip and increasing processing speed. However, the incessant demand for placing more number of CMOS devices on single-chip causes to reduce the device dimensions, leading to disturbing the switching characteristics of the transistors. Though, feature size of the transistor can be scaled down to nanometre regime by using scaling rules to minimize these disturbances. Subthreshold characteristics of CMOS devices degrade severely as moved to nanometre regime, leading to putting a limit on further scaling of conventional MOS transistors. But, consistent research and development are required for further scaling of technology to follow the International Technology Roadmap for Semiconductors (ITRS, 2013; Young, 1989). Therefore, it becomes essential to explore some alternative non-conventional CMOS devices. There are various nanoscale transistors reported by researches like Tunnel Field Effect Transistors (TFET) (Seabaugh & Zhang, 2010; Kim, 2010) impact ionization metal oxide semiconductor (I-MOS) (Gopalakrishnan, Griffin, & Plummer, 2002; Gopalakrishnan, Woo, Jungemann, Griffin & Plummer, 2002), FinFET (Raj, Saxena & Dasgupta, 2009), Nanowire FET (Scarlet, Ambika & Srinivasan, 2019; Sharma, Raj & Khosla, 2017), Nanotube FET (Tekleab, Tran, Sleight & Hidambarro, 2012; Tekleab, 2014), Carbon nanotube field-effect transistor (CNTFET), Tunnel CNTFET (Knock & Appenzeller, 2008; Shaker, Ossaimee, Zekry & Abouelatta, 2015) etc could be the solution for future CMOS applications.

2. CARBON NANOTUBE FIELD-EFFECT TRANSISTOR (CNTFET)

Carbon nanotube transistors may be considered as promising candidates for FETs due to exceptional electronic, mechanical and thermal properties of carbon nanotubes (CNTs) (Nardelli, Fattebert, Orlikowski, Roland, & Zhao, 2000; Avci, Rios, Kuhn & Young, 2011). CNTFET is having a similar device structure as Si-based MOSFET except for channel material, which is to be replaced by CNT of few nanometer diameters. Variable bandgap attributed to variable diameter of CNTFET makes it useful for different applications. In conventional MOSET, different materials have to be selected for different bandgaps. CNTFET requires low gate voltage as compared to conventional MOSFET (Pourfath, Mahdi, Kosina, & Selberherr, 2007; Koswatta, Nikonov, & Lundstrom, 2005). Therefore, CNTFETs are considered a highly promising candidate for future low power applications. According to their